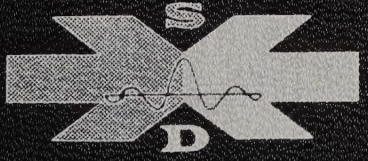
INSTRUCTION MANUAL

SD116

LOG FREQUENCY CONVERTER



SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO

SERIAL _____

INSTRUCTION MANUAL

SD116

LOG FREQUENCY CONVERTER

PATENT PENDING

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SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO

8911 Balboa Avenue, P.O. Box 671

San Diego, California 92112

Telephone: (714) 278-2501

TWX: 910-335-2022

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(Revised February 1969)

MODEL SD116 LOG FREQUENCY CONVERTER

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RECEIVING INSPECTION PROCEDURE

The Model SD116 Log Frequency Converter is shipped fully assembled, packed in a polystyrene case designed to protect it against all normal shipping hazards. Immediately upon receipt, inspect the exterior of the shipping case and note any visible damage. Keep all forms and invoices attached to the shipping case. Remove the instrument from the shipping case and test its functional operation in accordance with Section II of this manual. If shipping damage is apparent, file a claim with the carrier's claims agent and send a copy to Spectral Dynamics Corporation. Be sure to include the instrument name, model number, and serial number on all correspondence. Spectral Dynamics Corporation will advise the buyer what should be done; arrangements for repair or replacement will be made as applicable.

WARRANTY POLICY

All Spectral Dynamics products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain components listed in some of the operating manuals, for the specified period. We will repair or replace products which prove to be defective during the warranty period, providing the failure or damage has not been caused by misuse or abnormal operating conditions. Fuses and lamps are specifically excluded from warranty. If the malfunction or a portion thereof is determined by Spectral Dynamics Corporation to have been caused by misuse or abnormal conditions of operation, an estimate of cost to repair will be submitted to the purchaser for approval before beginning any repair work.

Liability under this warranty is limited to servicing and adjusting the instrument returned to the factory, with transportation charges prepaid by the purchaser. No other warranty is expressed or implied. We are not liable for consequential damages.

If any malfunction develops, notify Spectral Dynamics Corporation or its representative in your area, giving details of the problem, and the name, model and serial number of the equipment. Upon receipt of this information, service data or shipping instructions will be provided.

RETURN SHIPMENT PROCEDURE

On receipt of shipping instructions, forward the instrument prepaid via air freight to the factory or authorized repair station indicated on the instructions. Replace the instrument in its original shipping case, or surround with two to three inches of shock absorbing material and then pack it in a heavyweight cardboard box, wooden box, or other strong container.

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SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

The Model SD116 Log Frequency Converter is an all solid-state electronic, frequency to log d-c converter. The SD116 accepts any shape periodic waveform, sine wave to pulse with 10% or greater duty cycle, over the frequency range of 5 Hz to 20 kHz (in three decade intervals) and produces a d-c output of 0 to 1.0V proportional to the log of the frequency. The frequency being converted is also measured and displayed on a front panel meter calibrated in the three input ranges: 5 Hz to 5 kHz, 10 Hz to 10 kHz, and 20 Hz to 20 kHz.

1.2 BASIC OPERATION (See Figure 1-1.)

In the operate mode, the a-c input is applied to the limiter circuit which provides a constant amplitude square-wave signal to the frequency divider flip-flops. In the 5-Hz to 5-kHz range, the limiter output is gated through to the voltage ramp generators. In the 10-Hz to 10-kHz and 20-Hz to 20-kHz ranges, the limiter output is divided by 2 and 4 respectively; thus the input to the voltage ramp generators is always 5 Hz to 5 kHz.

Two out-of-phase voltage ramps are generated and are then alternately sampled for peak amplitude. The stored sample, a d-c voltage inversely proportional to the input frequency, is applied to a FET (field-effect transistor) amplifier. In turn, the FET produces a d-c control current (inversely proportional to frequency) which controls the log converter. Thus the log converter d-c output is proportional to the log of the input frequency. The d-c output varies from 0 to 1.00 volt proportional to the log of the input frequency for each operating range.

An internal 2-kHz oscillator and the line frequency are used to provide recorder (plotter) calibration points at an upper and a lower reference point.

1.3 SPECIFICATIONS

INPUT:

Frequency:	5 Hz to 20 kHz
Ranges:	5 Hz to 5 kHz, 10 Hz to 10 kHz, 20 Hz to 20 kHz
Waveform:	Any periodic waveform with >30% duty cycle
Impedance:	>40 kΩ
Voltage Amplitude:	Any level from 0.2V p-p to 100V p-p

OUTPUT:

Voltage:	Two simultaneously available log d-c outputs with nominal sensitivities of 333-1/3 mV and 33-1/3 mV per decade (no linear d-c output):

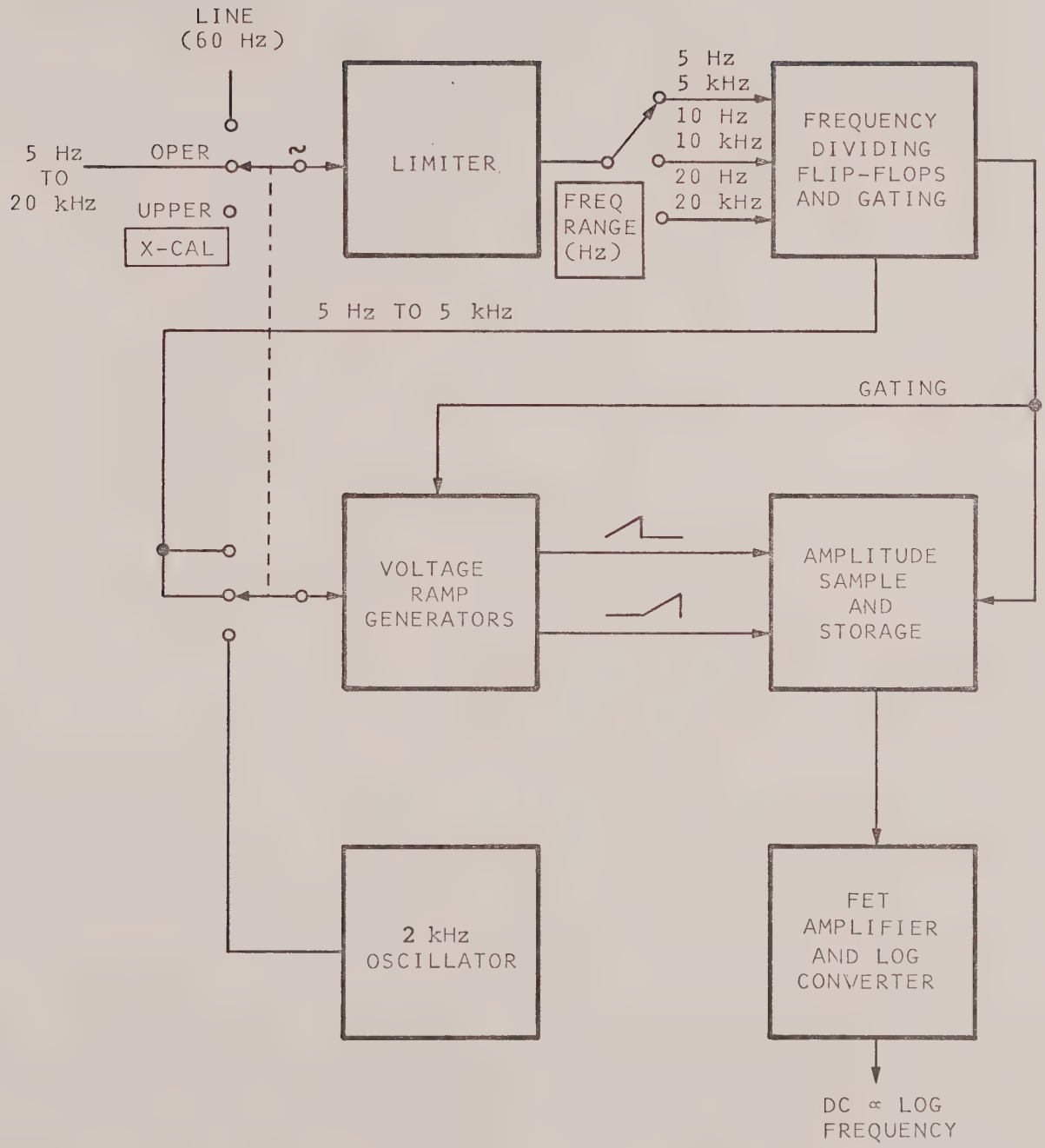


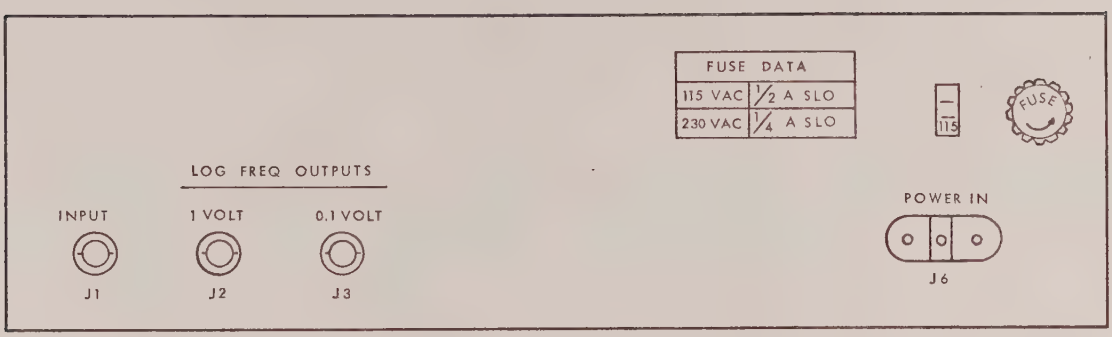
Figure 1-1. Simplified Block Diagram of Log Frequency Converter

1.3 SPECIFICATIONS (Cont'd)

Voltage (cont'd):	5,000 Hz = 100 mV 500 Hz = 66-2/3 mV 50 Hz = 33-1/3 mV 5 Hz = 0	For 5-Hz to 5-kHz range, proportional in upper two ranges
Ripple:	Less than 1% of full-scale output voltage level.	
Impedance:	50Ω nominal at 0.1V output (short-circuit proof) 500Ω nominal at 1V output (short-circuit proof)	
Accuracy:	2% of frequency ±0.002% of full-scale frequency range.	
RESPONSE TIME:	Inversely proportional to frequency: ≈500 ms at 5 Hz, and ≈25 ms at 20 kHz	
CALIBRATION:	Calibration of recorder facilitated by two front panel selected frequencies: Line frequency (60 Hz) for lower reference point, and internal oscillator provides upper frequency reference point 2/5 full scale of range selected.	
INPUTS/OUTPUTS:	INPUT and OUTPUT connectors on front panel are in parallel with respective INPUT and 1 VOLT LOG FREQ OUTPUT connectors on rear panel; 0.1 VOLT LOG FREQ OUTPUT on rear panel only.	
POWER:	115-125/210-250 Vac, 50/60 Hz, at ≈6W	
DIMENSIONS:	Height.....3½" (8,89 cm) Width.....19" (48,3 cm) Std. panel Depth.....14" (35,6 cm) w/o Connectors Shipping Weight....8½ lbs (3,85 kg)	

1.4 FRONT AND REAR PANELS

Figures 1-2 and 1-3 show the instrument front and rear panels respectively, and describe the function of each control, switch, meter, and connector.



INPUT (J1)

Provides input connection at rear of instrument when used in a system (rack-mounted in cabinet); connected in parallel with INPUT connector on front panel. (See Figure 1-2.)

LOG FREQ OUTPUTS

1 VOLT (J2) - Connected in parallel with OUTPUT connector on front panel. (See Figure 1-2.)

0.1 VOLT (J3)- Provides output d-c voltage of 0 to 0.1 volt proportional to the log of the input frequency over the selected range.

POWER IN

Accepts 3-wire plug and cable (supplied) for applying 115/230 Vac, 50-60 Hz primary input power. Center terminal is chassis ground. Uses Belden No. 17258 cable (as used on most Hewlett-Packard instruments, and obtainable from normal sources of H-P parts).

230/115 switch

Facilitates changeover of primary power input circuit for either 230V or 115V operation. Proper input power to be applied shows in window; screwdriver blade slot is up for 115V operation and down for 230V operation.

FUSE

Contains 3AG type, SLO-BLO fuse; ½A for 115V operation or ¼A for 230V operation.

Figure 1-3. Rear Chassis Description

SECTION II

OPERATION

2.1 INTRODUCTION

This section provides instructions for operating the Model SD116 Log Frequency Converter. This instrument provides a d-c output, 0 to 1V, that is proportional to the log of the input signal frequency.

2.2 CONTROLS, INDICATORS, AND CONNECTORS

All controls, indicators, and connectors are identified and their operations are described on Figures 1-2 and 1-3 in Section I of this manual.

2.3 TURN-ON PROCEDURE

a. Check rear chassis 230/115 switch for proper input line voltage.

b. Plug power cord (Belden No. 17258 supplied) into POWER IN receptacle on rear of chassis and connect to primary power receptacle.

c. Press POWER switch/indicator on front panel; it should glow red indicating power is on.

NOTE

Allow at least 5 minutes for the instrument to warm up and stabilize.

2.4 OPERATING INSTRUCTIONS

a. Connect the frequency signal source to front panel INPUT (J4) or rear chassis INPUT (J1).

b. Connect recorder to applicable rear chassis LOG FREQ OUTPUTS connector, 1 Volt (J2) or 0.1 VOLT (J3). The front panel OUTPUT connector is in parallel with 1 VOLT (J2) rear chassis connector.

c. On the front panel, set the FREQ RANGE switch to the desired frequency range. Ensure that the X-CAL switch is set to OPER.

2.5 RECORDER X-AXIS CALIBRATION

When the SD116 is used in a mechanical impedance (MZ) measuring system, the dc ∝ log frequency is normally connected to the Master Control Unit (SD23A-2) for use in MZ computations and to the recorder X-axis input. The recorder X-axis can be calibrated as follows:

a. On the SD116 front panel, set the X-CAL switch to LINE. Adjust recorder controls to place X-axis pen over the 60-Hz lower reference point.

b. Set the X-CAL switch to UPPER, and adjust the recorder GAIN control to place the X-axis pen over the upper frequency reference point (2 kHz, 4 kHz, or 8 kHz).

c. Repeat steps a. and b. as required to compensate for any interaction.

d. After calibration is complete, return the X-CAL switch to OPER.

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

This section describes the theory of operation of the Model SD116 Log Frequency Converter.

3.2 BLOCK DIAGRAM DISCUSSION

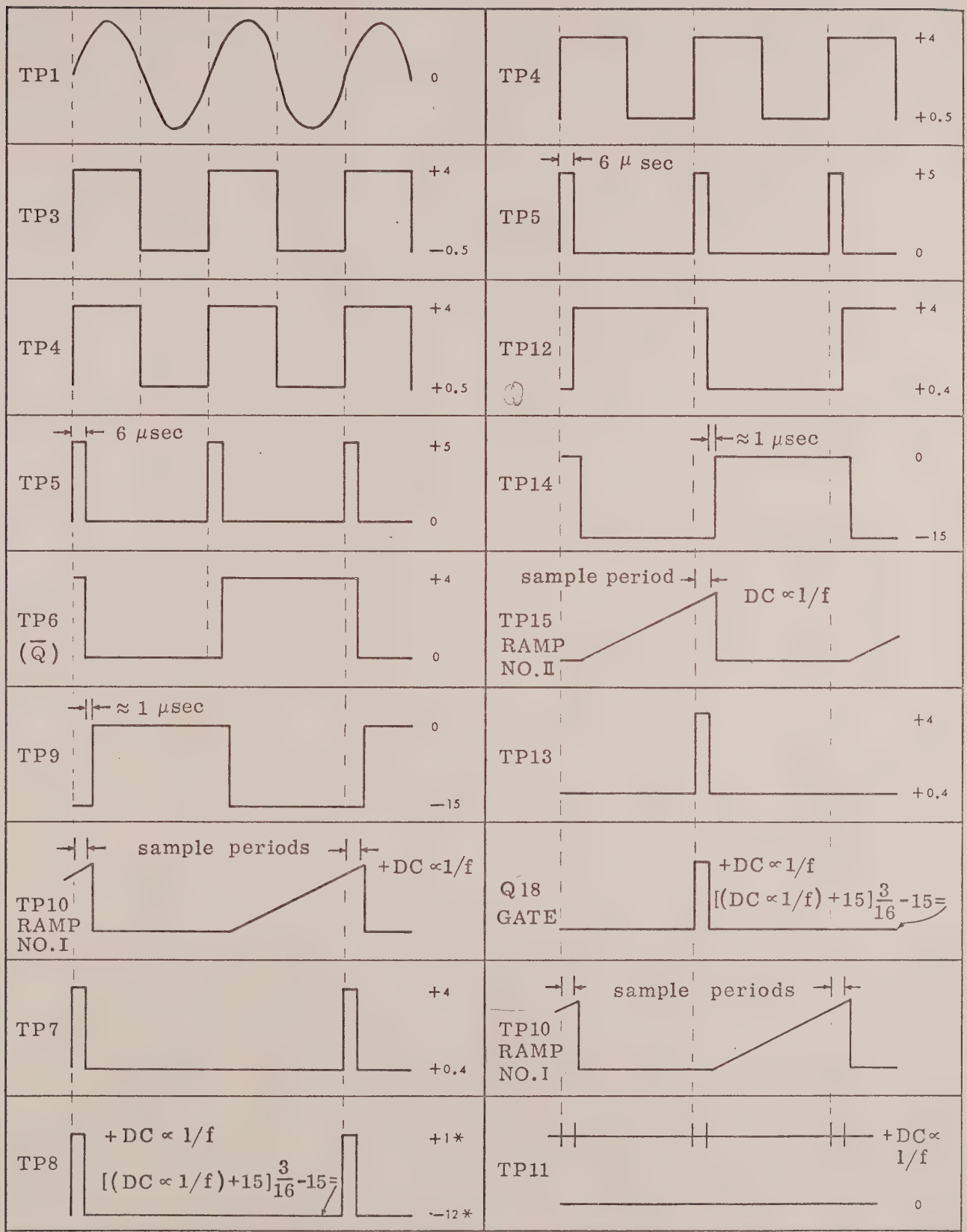
Throughout the following discussion, refer to Figures 3-1 and 3-2. Figure 3-2 is a functional block diagram of the log frequency converter circuit. The input and output of each main subcircuit is identified by a test point; the associated waveforms are shown in Figure 3-1.

The waveforms in the first column of Figure 3-1, from top to bottom, depict the development of the input sine wave at TP1 to ramp No. I at TP10, followed by its associated sample/transfer pulses (TP7 and TP8). For ease of comparison in timing, TP4 and TP5 have been repeated at the top of the second column. The waveforms in this column depict the development of ramp No. II, followed by its associated sample/transfer pulses (TP13 and Q18-G). Then TP10 is repeated to show the combination of TP10 and TP15 to form TP11 (+DC $\propto$ 1/f).

For this discussion, assume an input signal of 1 kHz, 0.5V p-p, sine wave. The X-CAL switch is set to OPER and the FREQ RANGE switch is set to 5-5K.

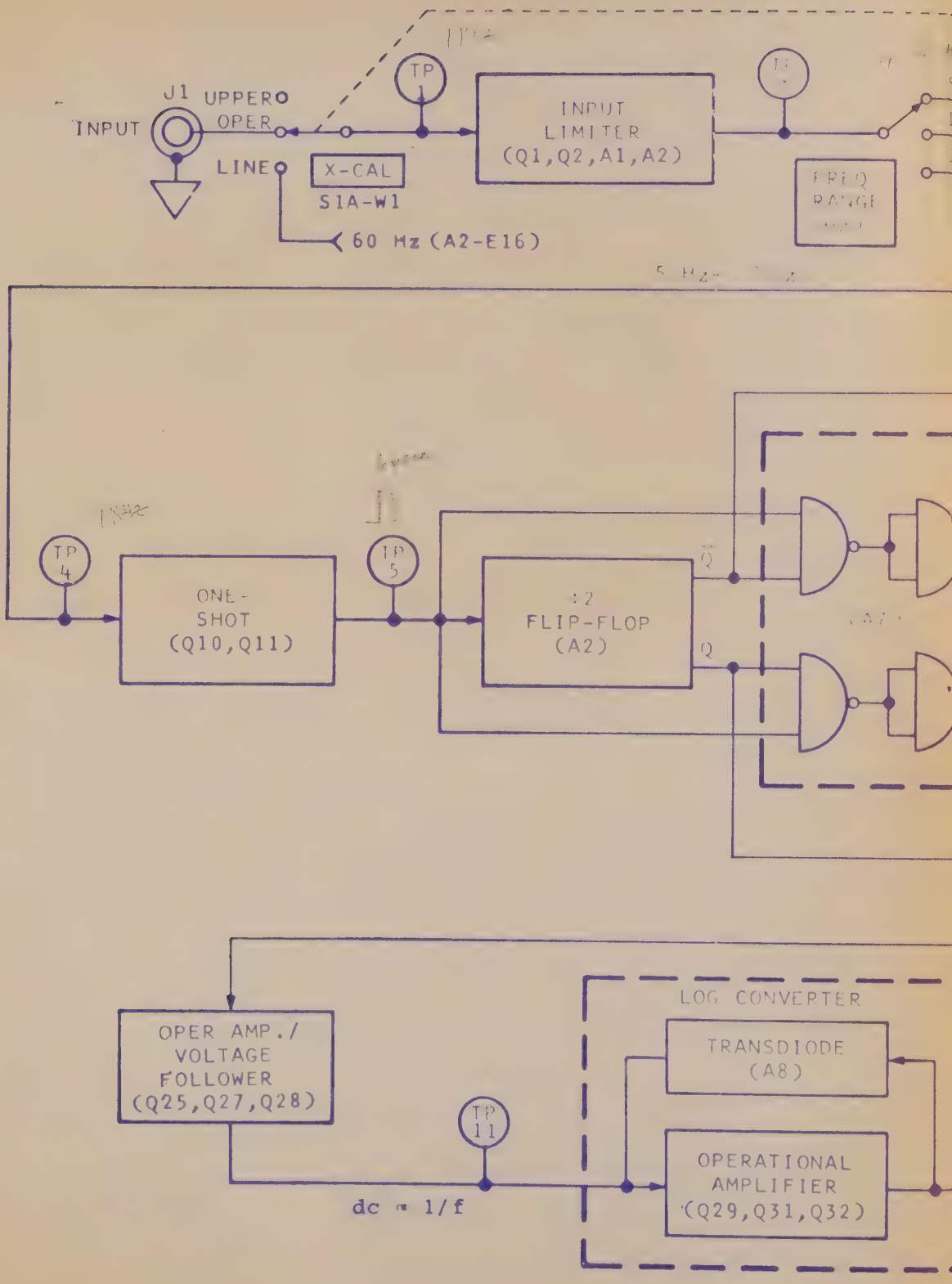
The 1-kHz signal applied at INPUT (J1) is routed through X-CAL switch S1A to the input limiter. Here the 1-kHz sine wave is converted to a constant-amplitude ($\approx$4.5V p-p) 1-kHz square-wave signal for application to the frequency dividing flip-flops. With the FREQ RANGE switch set to 5-5K, the 1-kHz signal is routed through to the one-shot; therefore, the signal at TP4 is a 1-kHz square-wave signal, $\approx$4.5V p-p. Note that if the FREQ RANGE switch was set to 10-10K or 20-20K, a frequency division of 2 or 4 would be done to produce a 500-Hz or 250-Hz signal respectively at TP4. The log frequency converter circuitry between TP4 and TP18 always operates over the frequency range 5 Hz to 5 kHz; therefore frequency division is performed on all signals above 5 kHz. The divisor (2 or 4) is determined by the setting of the FREQ RANGE switch.

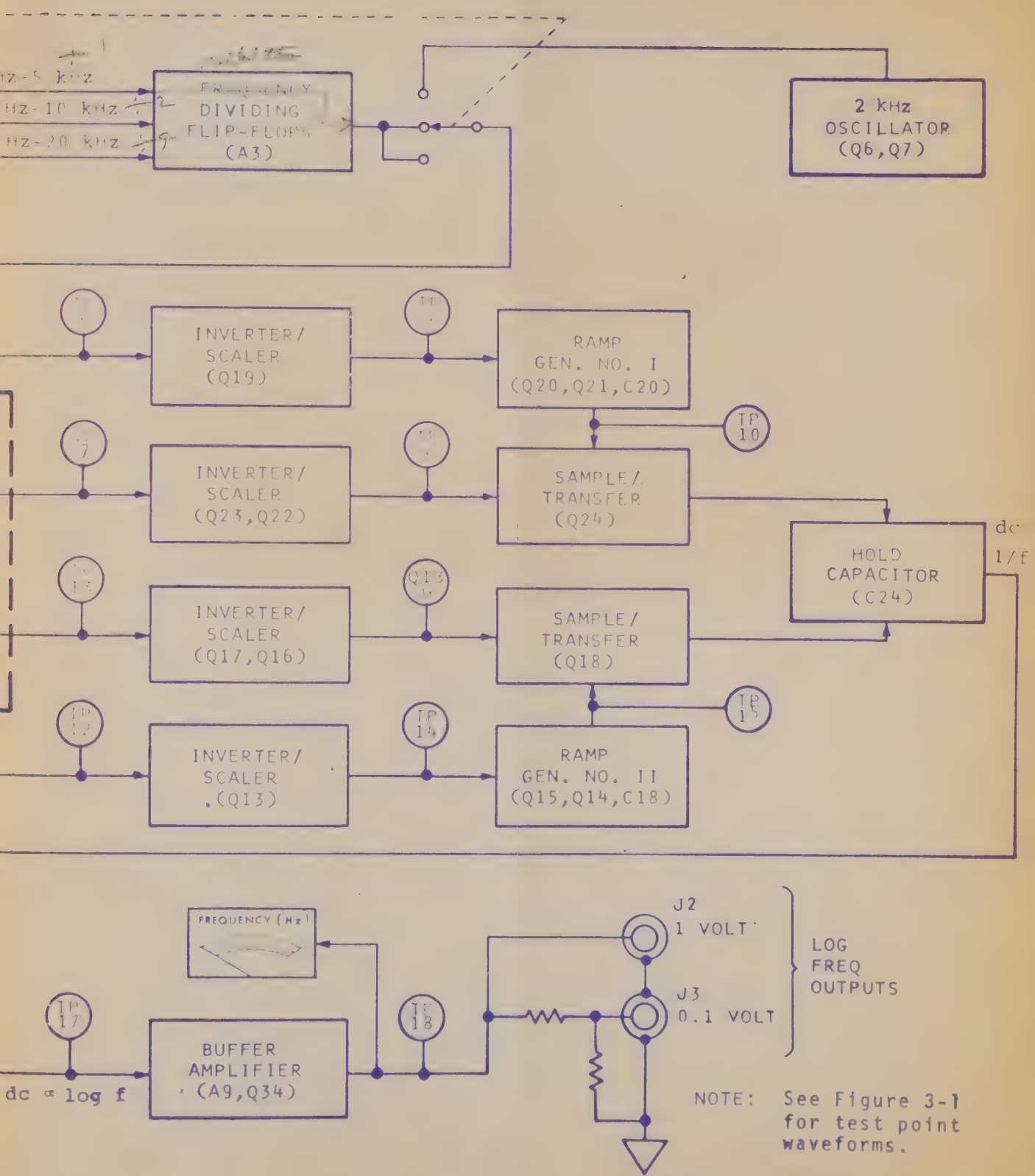
See Figure 3-2 and note the placement of the X-CAL switch in the overall circuit. This switch facilitates recorder calibration at the line frequency (60 Hz) and an upper frequency reference point of any range selected. With X-CAL set to UPPER, the 2-kHz oscillator signal applied to the one-shot at TP4 produces a LOG FREQ OUTPUT of 0.867 Vdc. With S9A set to LINE, the 60-Hz ac is routed through, divided by two, or divided by four as determined by the FREQ RANGE switch setting, and produces a dc $\propto$ log frequency 60 Hz, the amplitude being relative to the particular range. In like manner, all input frequencies are processed to produce a dc $\propto$ log input frequency, the amplitude being



* Voltages from formulas, f at TP4 = 50 Hz.

Figure 3-1. Logic Timing Diagram


J1 UPPER
INPUT
OPER
LINE
X-CAL
S1A-W1
60 Hz (A2-E16)
TP
INPUT LIMITER (Q1,Q2,A1,A2)
FREQ RANGE
TP 4
ONE-SHOT (Q10,Q11)
TP 5
÷2 FLIP-FLOP (A2)
Q̄
Q
OPER AMP./ VOLTAGE FOLLOWER (Q25,Q27,Q28)
TP 11
dc ∝ 1/f
LOG CONVERTER
TRANSDIODE (A8)
OPERATIONAL AMPLIFIER (Q29,Q31,Q32)



NOTE: See Figure 3-1 for test point waveforms.

Figure 3-2. Functional Block Diagram Model SD116 Log Frequency Converter

relative to 1 Vdc as determined by the particular FREQ RANGE switch setting.

The one-shot produces 6-μs pulses at TP5 which drive the ÷2 flip-flop. The two flip-flop outputs, $\overline{Q}$ and Q, along with the 6-μs pulses (TP5) are used to develop alternately the two voltage ramps and transfer their peak amplitude (dc ∝ 1/f) into hold capacitor C24.

$\overline{Q}$ (TP6) is inverted and scaled to form TP9 which is used to develop ramp No. I. $\overline{Q}$ and TP5 are ANDed (in series NAND gates of element A7) to form TP7. TP7 is scaled to produce TP8 which samples the peak amplitude of ramp No. I (TP10) and transfers it to hold capacitor C24.

Q (TP12) is inverted and scaled to form TP14 which is used to develop ramp No. II. Q and TP5 are ANDed in element A7 to form TP13. TP13 is scaled to produce voltage at Q18-gate which samples the peak amplitude of ramp No. II (TP15) and transfers it to hold capacitor C24.

Compare the timing relationships of TP1, TP4, TP15, and TP10, and note that hold capacitor C24 is pulsed once each cycle to maintain its charge equal to dc ∝ 1/f. The component values have been chosen to accommodate rapid frequency changes at either end of the input spectrum, never requiring more than two input frequency cycles (at TP4) to charge C24 to dc ∝ 1/f.

The voltage charge in C24 is sensed by a high-impedance input FET (field effect transistor) operational amplifier circuit, and then buffered by a voltage follower for application to the log converter.

The voltage at TP11 (dc ∝ 1/f) controls the current flow into the log converter. The log converter is basically an operational amplifier with its gain controlled by the feedback current through a transdiode. Because of the nonlinear characteristics of the transdiode, the current flowing through it develops a new voltage that is proportional to the logarithm of the input voltage. (Its output is also inverted.) Therefore, the output of the log converter at TP17 is a d-c voltage proportional to the log of the input frequency.

The dc ∝ log frequency is buffered and routed to LOG FREQ OUTPUT connector J2. A precision 10:1 attenuator provides a 0 to 0.1V output at J3.

3.3 THEORY OF OPERATION

The following subparagraphs describe in detail the circuits of the log frequency converter. Because digital logic circuitry is used, a brief description of the logic elements and their operation is given in paragraph 3.3.1. Throughout the circuit descriptions, refer to Figures 3-1 and 3-2, and to the schematic diagram located at the back of this manual.

NOTE

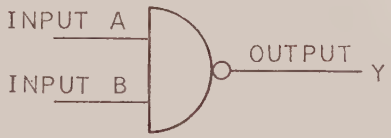
Because all parts referenced throughout the following circuit descriptions are located on circuit card A1 (except switches S1A and S2A and the power supply components which are identified as such), for the sake of clarity the prefix "A1" has been deleted from all parts designators.

3.3.1 Digital Logic Elements

Four standard types of Texas Instrument Series 74 digital logic elements are used as follows: SN7473N Dual J-K Master-Slave Flip-Flop, SN7400N Quadruple 2-Input Positive NAND Gate, SN7420N Dual 4-Input Positive NAND gate, and SN7472N J-K Master-Slave Flip-Flop, Figure 3-3 shows the logic symbol and element internal wiring connections for each type, along with their associated truth table.

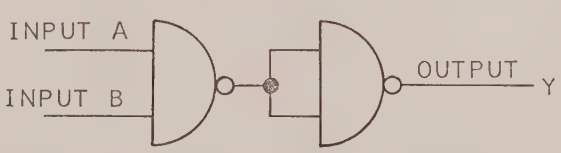
Positive logic is used throughout the NAND gating circuitry: i.e., a logic "1" or "enable" is +2.4V to +5.5V (4V nominal) or an open circuit; a logic "0" or "disable" is 0V to 0.4V or ground.

The operation of a typical NAND gate is as follows:



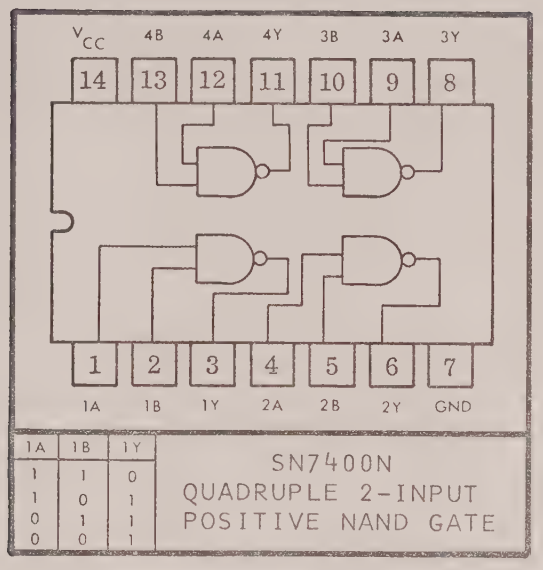
Using positive logic, both inputs A and B must be a logic "1" to produce a logic "0" at output Y. All other combinations of inputs produce a "1" at Y.

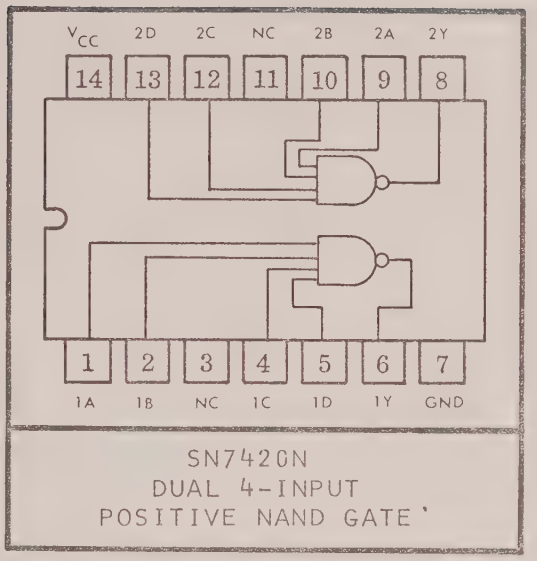
When two NAND gates are connected in series as shown below, the total circuit performs the AND function as follows:

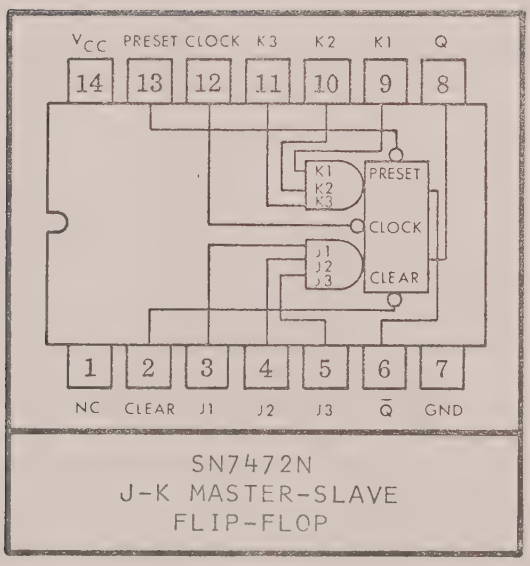


Because the second NAND gate inverts its inputs, using positive logic, both inputs A and B must be a logic "1" to produce a logic "1" at output Y. All other combinations of inputs produce a "0" at Y.

Three J-K flip-flop circuits are used; each operates as follows: As shown in the waveform timing diagram for the J-K flip-flop, the outputs Q and $\overline{Q}$ change logic state only on the negative-going CLOCK input; i.e., when the CLOCK input changes from a "1" to a "0".


V_{CC} 4B 4A 4Y 3B 3A 3Y
14 13 12 11 10 9 8
1 2 3 4 5 6 7
1A 1B 1Y 2A 2B 2Y GND
1A 1B 1Y
1 1 0
1 0 1
0 1 1
0 0 1
SN7400N
QUADRUPLE 2-INPUT
POSITIVE NAND GATE





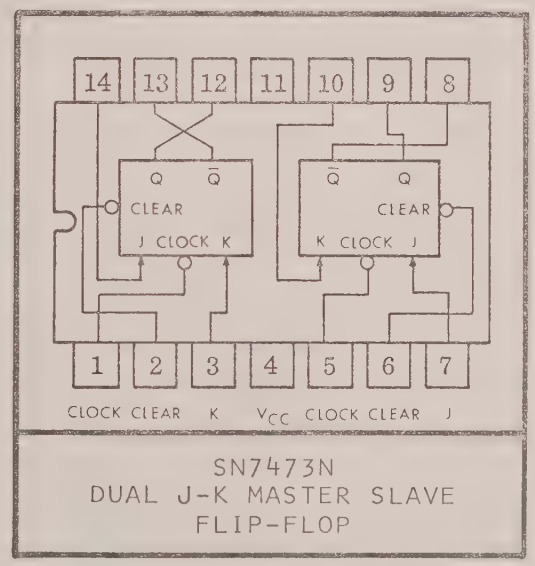
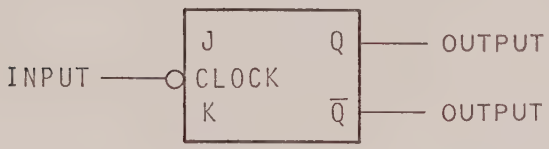
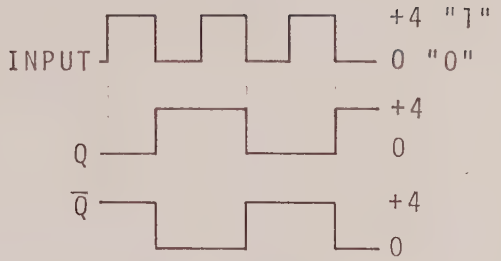


Figure 3-3. Digital Logic Elements





3.3.2 Input Limiter

The input limiter circuit will accept any shape periodic waveform, sine wave to pulse with 30% or greater duty cycle, over the frequency range of 5 Hz to 20 kHz, with an amplitude from 0.2V to 100V p-p. Its output (TP3) is a constant amplitude square-wave signal, ≈4.5V p-p, whose frequency is in phase with and equal to the input (TP1).

Transistors Q1 and Q2, element A1, and diodes CR1 and CR2 are connected as an operational amplifier. This amplifier operates linearly over the input voltage range; feedback via CR1 and CR2 prevents input overloading. The output of element A1 is a square wave signal, nominally 1V p-p, that drives element A2.

Element A2 operates as a differential comparator with (+) input pin 2 referenced to ground. When (-) input pin 3 is 1 mV or more below ground, the output (TP3) is ≈+4V; when pin 3 is 1 mV or more above ground, the output is ≈-0.5V.

3.3.3 Range Switching (Frequency Division)

The log frequency converter circuitry, between TP4 (at input to Q10) and TP18 (dc ∝ log frequency), operates over the frequency range of 5 Hz to 5 kHz. Therefore, INPUT frequencies in the 10-Hz to 10-kHz range are divided by two, and frequencies in the 20-Hz to 20-kHz range are divided by four. This frequency division is accomplished by dual flip-flop element A3 in conjunction with three 2-input NAND gates in element A4, one 4-input NAND gate in element A5, and FREQ RANGE switch S2A. (See Figure 3-4.)

In the 5-Hz to 5-kHz range, S2A grounds (applies logic "0") A4-5 and A4-10. In this condition, A4-8 and A4-6 are logic "1"s, enabling A5-5 and A5-4 respectively. Because A4-2 is enabled (open or logic "1"), the INPUT passes through and is inverted by A4-2 and A4-3. Because A5-5 and A5-4 are enabled ("1"), A5-2 accepts the output of A4-3 and inverts it, and thus the output of A5-6 is the same frequency as the INPUT.

In the 10-Hz to 10-kHz range, S2A-W1 grounds A4-10, making A4-8 a "1" enabling A5-5. S2A-W2 grounds (disables) A4-2 making A4-3 a "1" to enable A5-1 and -2. Note that with A4-2 disabled, the INPUT at A4-1

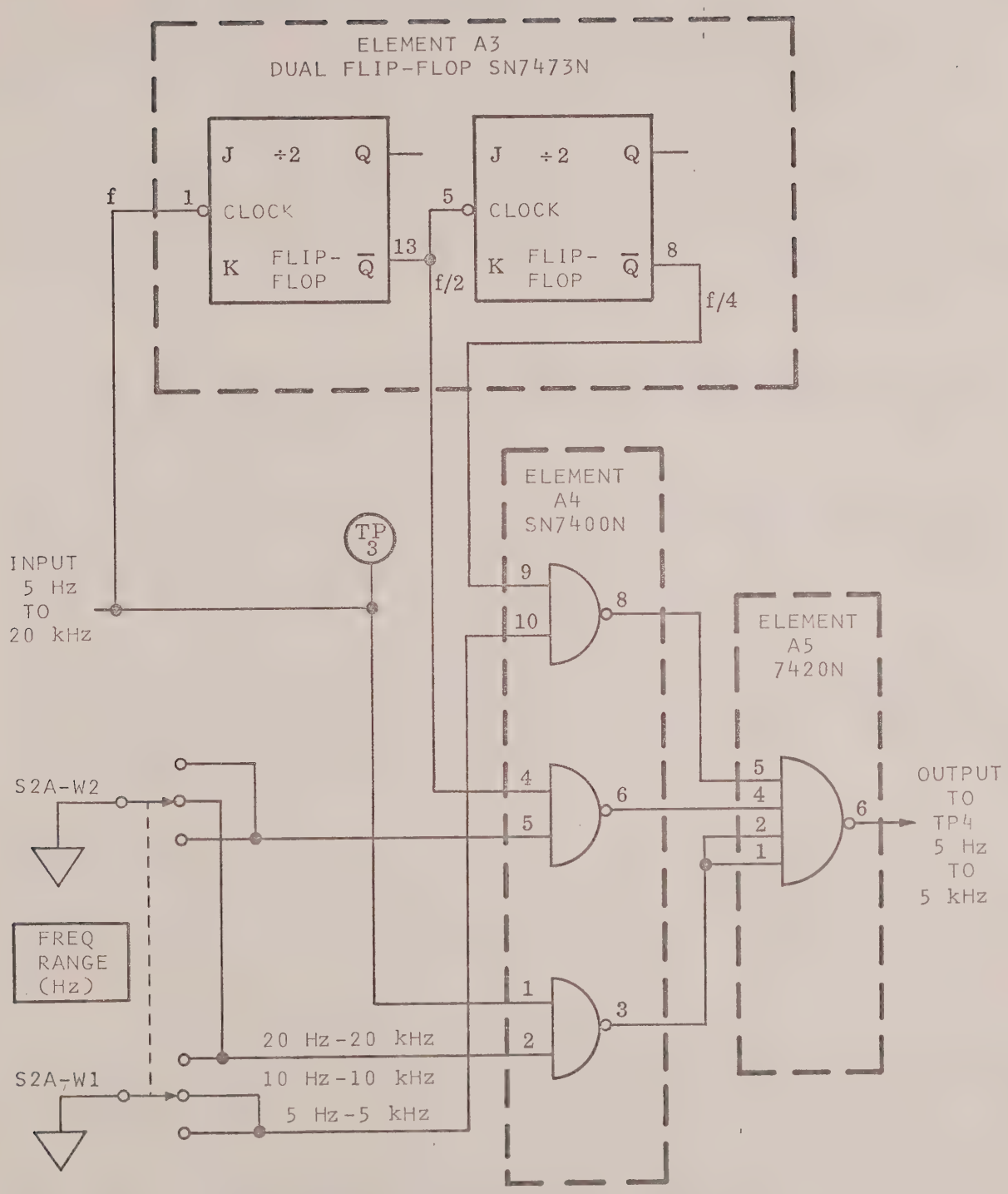


Figure 3-4. Logic Diagram of Range Switching (Frequency Division) Circuitry

3.3.3 Range Switching (Frequency Division) (Cont'd)

has no affect. A4-5 is enabled (open or logic "1"); therefore f/2 from A3-13 can pass through A4-4 to A4-6, and subsequently through A5-4 to A5-6. The output frequency at A5-6 is now one-half the input frequency.

In the 20-Hz to 20-kHz range, S2A disables A4-5 and A4-2; A4-10 is open (enabled). In this condition, A4-6 and A4-3 are "1"s enabling A5-4 and A5-2, -1. A4-8 (A5-5) changes state inversely as A4-9. Therefore, only f/4 from A3-8 can pass through A4-9 to A4-8, and subsequently through A5-5 to A5-6. The output at A5-6 is now one-fourth the INPUT frequency.

3.3.4 X-CAL

The X-CAL switch (S1A) facilitates recorder calibration at two frequencies: LINE frequency (60 Hz) and an upper frequency reference, 2/5 full scale range selected.

With X-CAL switch S1A set to LINE, approximately 75 volts, 60-Hz ac from the power supply is applied through S1A-W1 to the limiter input (TP1). Therefore, a d-c voltage proportional to 60 Hz is provided at the output (TP18). The amplitude is relative to the FREQ RANGE switch setting; i.e., the dc $\propto$ log 60 Hz is 3.6V, 2.6V, and 1.6V (±24 mV) for FREQ RANGE settings 5-5K, 10-10K, and 20-20K respectively.

With X-CAL switch S1A set to UPPER, an internal 2-kHz multivibrator is activated and its output is applied directly to the one-shot input (TP4, base of Q10). Because the upper frequency limit of the circuitry from this point to the output (TP18) is 5 kHz (refer to paragraph 3.3.3), the dc $\propto$ log frequency will be 0.867V at TP18 for any setting of FREQ RANGE switch S2A.

The 2-kHz multivibrator comprises Q6, Q7, CR3, C12, C13, and R23 through R28. With S1A set to UPPER, +5V from emitter of Q8 (voltage regulator) is routed through A5-J to S1A-W2 (UPPER), through A5-K, R27, and R26 to the base of Q7. In this condition, the multivibrator oscillates at 2 kHz. The 2-kHz output at TP16 is routed through A5-6, S1A-W3 (UPPER), and A5-7 to the one-shot input at TP4.

3.3.5 One-Shot and ÷2 Flip-Flop

See Figure 3-2 and note that the one-shot and ÷2 flip-flop generate the basic pulses used to develop the two ramps, and then transfer their peak amplitude (dc $\propto$ 1/f) into the hold capacitor for subsequent log conversion.

Q10 and Q11 operate as a collector-coupled one-shot multivibrator; Q12 determines the pulse output voltage swing from 0V to +5V. See Figure 3-1 and note that each positive-going zero-crossing input (TP4) produces a 6-µs pulse (TP5). The 6-µs pulses drive ÷2 flip-flop element A6. The outputs of element A6 (Q and $\overline{Q}$) change state only on the negative-going input; i.e., at one-half the TP4 input frequency.

3.3.5 One-Shot and ÷2 Flip-Flop (Cont'd)

Therefore Q and $\overline{Q}$ are alternately in a positive (+4V) state for the time equal to the period (1/f) of the input frequency at TP4. This technique is the basis for developing the two ramps, alternately, with their peak amplitude dc ∝ 1/f.

The output of the one-shot (TP5) is NANDed with $\overline{Q}$ (element A6-6) in element A7 (pins 10 and 9). The NANDed output at A7-8 is inverted by NAND element A7-13, -12, and -11. This overall connection performs the AND function; i.e., the output at A7-11 (TP7) is a logic "1" only when TP5 and $\overline{Q}$ are positive (logic "1" level). This train of ≈6-μs pulses at TP7 is subsequently scaled to produce TP8 which controls the sampling of ramp No. I peak amplitude (described in paragraph 3.3.6.1).

The output of the one-shot (TP5) is also NANDed with Q (element A6-8) in element A7 (pins 1 and 2), and inverted by element A7-4, -5, and -6. This logic produces the waveform at TP13. This train of ≈6-μs pulses at TP13 is subsequently scaled to produce the input to Q18-gate which controls the sampling of ramp No. II peak amplitude (described in paragraph 3.3.6.2).

3.3.6 Ramp Generators

3.3.6.1 Ramp No. I

Q19 inverts and scales the +4V to +0.4V waveform at TP6 to the 0V to -15V waveform at TP9 (collector of Q19 and gate of Q20). With 0V input to Q20 gate, Q20 source-to-drain resistance is about 30 ohms, which shunts (discharges) ramp storage capacitor C20. When Q20 gate (TP9) goes to -15V, the source-to-drain resistance is almost infinite, and C20 charges linearly as supplied by Q21, a constant current source. Thus, a linear ramp (TP10) is developed during the period of one cycle of the input frequency (at TP4).

When TP9 goes to 0V, C20 is again shunted and discharged. Note, however, that just prior to this point, the ramp amplitude is proportional to the period of the TP4 input frequency, or, is proportional to the reciprocal of frequency (1/f).

3.3.6.2 Ramp No. 2

Q13 inverts and scales the +4V to +0.4V waveform at TP12 to 0V to -15V at TP14 (collector of Q13 and gate of Q15). When input to Q15 gate is 0V, the source-to-drain resistance is approximately 30 ohms, which shunts (discharges) ramp storage capacitor C18. When input to Q15 gate goes to -15V, the source-to-drain resistance is almost infinite, thus C18 charges linearly as supplied by Q14, a constant current source. Thus, a linear ramp (TP15) is developed during the period of one cycle of the input frequency (at TP4).

When TP14 goes to 0V, C18 is shunted and discharged. Note, however, that just prior to this point, the ramp amplitude is proportional to the TP4 input frequency period, or is proportional to the reciprocal of frequency (1/f).

3.3.7 Sample, Transfer, and Hold

3.3.7.1 Ramp I

Observe waveform TP7 and note that its positive-going leading edge occurs about 6 μs before the end of the ramp peak. This +4V to +0.4V waveform (TP7) is scaled by Q23 and Q22 to the -15V to 0V waveform at TP8, which is applied to the gate of Q24. Therefore, Q24 is turned on and transfers the last 6 μs of peak ramp voltage from C20 into C24, the "hold capacitor." Note that waveforms TP9 and TP10 are both delayed approximately 1 μs; this is caused by C19 (base to emitter of Q19). This 1-μs delay allows the sampling pulse (TP8) to turn off Q24 about 1 μs before Q20 turns on and discharges C20.

3.3.7.2 Ramp II

During the last 6 μs of each alternate TP4 input cycle, Q18 is turned on and transfers the peak ramp voltage from C18 into "hold capacitor" C24. Waveform TP13 is developed by ANDing TP5 (one-shot output) and TP12 (Q output from A6-8) in series NAND gates A7 (terminals 1 through 6). Waveform TP13 (4V to 0.4V) is scaled by Q17 and Q16 to the -15V-to-0V waveform applied to Q18-gate. Note that waveforms TP14 and TP15 are both delayed approximately 1 μs; this is caused by C17 (base to emitter of Q13). This 1-μs delay allows the sampling pulse at TP13 to turn off Q18 about 1 μs before Q15 turns on and discharges C18.

3.3.8 D-C Buffer Amplifier

The voltage (dc $\propto$ 1/f) stored in "hold capacitor" C24 is buffered by an operational follower amplifier for application to the log converter circuit. This amplifier comprises differential pairs Q25 and Q27, and emitter follower Q28. Q26 provides a constant current source for Q25. Having greater than 10^9 ohms input impedance, the input gate of Q25 offers almost no load to C24.

The 24V supply for Q25 and Q27 is developed from the 38V unregulated input at pin M. The 38V is filtered by R72, C25, and R73, and then regulated to +24V by 9V zener diode CR12 which is referenced to the +15V regulated supply.

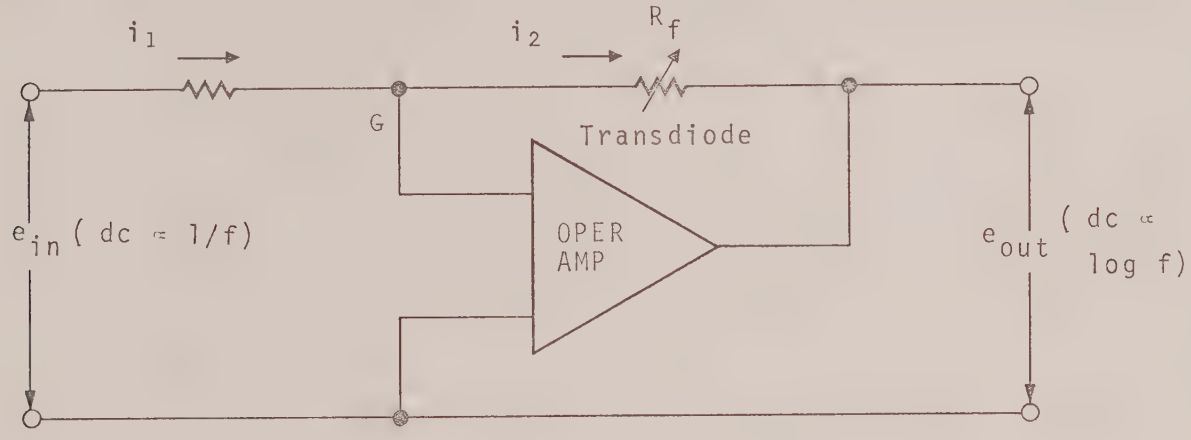
The small high-frequency "spikes" shown on TP11 waveform (output of Q28) are switching transients caused by Q18 and Q24; they are non-affective. The output of Q28 (dc $\propto$ 1/f) is fed to the log converter circuit.

3.3.9 Log Converter

The log converter circuit consists of an operational amplifier (differential pairs Q29 and Q31, and emitter follower Q32), a transdiode (diode-connected transistor, element A8 terminals 2, 3, and 4), and associated circuitry. Q30 provides a constant current source for Q29.

Q29, Q31, and Q32 operate as a conventional operational amplifier except that the overall gain is controlled by the feedback through

transdiode element A8. Because the impedance of a transdiode varies inversely and logarithmically as the current forced through it, the overall gain of the operational amplifier is caused to vary inversely and logarithmically. Therefore, because the gain of an operational amplifier is equal to the feedback impedance divided by the input impedance (gain = $\frac{R_{FB}}{R_{IN}}$), and the transdiode impedance is varying inversely and logarithmically to the input, the voltage developed at the output is proportional to the log of the input. This function is illustrated as follows:



Q29, Q31 and Q32 operate as a conventional operational amplifier with a transdiode substituted to R_f. Therefore, to maintain ground potential at the summing junction (point G), the input current (i_1) must equal the output current (i_2). Because R_f is a transdiode (whose impedance varies logarithmically as the current passed through it), i_2 (= i_1) is proportional to the antilog of e_{out}. Also, because $i_2 = i_1 = e_{in}/R_{in}$, e_{in} is proportional to the antilog of e_{out}; or e_{out} is proportional to the log of e_{in}. This logic is given in brief mathematical form as follows:

$$i_2 \propto \exp e_{out}$$

or

$$e_{out} \propto \log i_2$$ (from basic diode equation, neglecting temperature changes)

but

$$i_2 = i_1 = e_{in}/R_{in}$$

therefore

$$e_{out} \propto \log e_{in}/R_{in} \propto \log e_{in}$$

or

$$e_{out} \propto \log e_{in}$$

3.3.9 Log Converter (Cont'd)

The transdiode element is contained in an oven, along with a second diode-connected transistor that has identical operating characteristics. The DC ∝ log f (output of Q32 at junction of R91, C29, and A8-10) passes through this second diode which provides an offset to cancel the "constant of proportionality" (K) of the log converter. The voltage at TP17 is therefore equal to log f. This voltage is applied to the output buffer amplifier.

Note that because the log converter diode and offset diode are on the same "chip" in the same oven, both are equally affected by any temperature change and thus compensate each other equally.

3.3.10 Output Buffer Amplifier

The output buffer amplifier consists of element A9, emitter follower Q33, and associated circuitry, connected as an operational amplifier. CR14 and CR15 provide input overload protection. The overall gain is approximately 40. Q33 provides ample current at the output connectors to drive external recording equipment. The output is short-circuit proof with a nominal output impedance of 500 ohms.

3.3.11 Power Supply

Power supply card A2 provides all circuit d-c operating voltages (+15V, -15V, and ≈+38V).

The primary power input applied at POWER IN connector J5 pin 3, is routed through fuse F1, contacts 1 and 2 of POWER switch/indicator S3, to primary of T1 on card A2. The setting of switch S4 connects the T1 primary windings in parallel for 115 volt operation or in series for 230 volt operation.

Both the -15V and +15V supplies use conventional solid-state diode rectification and electronic voltage regulation circuitry. Note, however, that the regulation of the +15V supply is slaved to the -15V output via resistors R3 and R4 (on card A2). This connection causes the two supplies to track each other; i.e., their outputs, although opposite in polarity, are always equal in amplitude.

SECTION IV

CALIBRATION AND MAINTENANCE

4.1 INTRODUCTION

This section contains calibration procedures and maintenance instructions for the Model SD116 Log Frequency Converter. The instrument has been calibrated at the factory prior to shipment and should remain calibrated indefinitely. However, because of possible amplifier gain changes over long periods of operation, and when parts are replaced, the calibration should be checked periodically and adjustments made as necessary in accordance with the procedure of paragraph 4.2. If proper operation cannot be achieved, refer to paragraph 4.3 for troubleshooting techniques and general maintenance information. The test equipment required for maintenance of the Log Frequency Converter is listed in Table 4-1; test equipment having equal or better characteristics may be substituted.

Before calibrating or troubleshooting, the technician is advised to study carefully the theory of operation of Section III, and Figures 1-2 and 1-3 in Section I which describe the front and rear panel controls, indicators, and connectors. See also the schematic and circuit card component layout drawing located in the back of this manual. For parts replacement information, refer to paragraph 4.4

A complete and detailed calibration procedure, based on the factory final checkout procedure, is given in paragraph 4.5.

Table 4-1. TEST EQUIPMENT REQUIRED.

Name	Model No.	Manufacturer
Digital Voltmeter	3440A	Hewlett-Packard
Frequency Counter	5223L	Hewlett-Packard
Lab Amplifier (G = 10)	-----	Spectral Dynamics
Oscilloscope	561A1	Tektronix
Time Base Plug-In	Type 67	Tektronix
Wide-Band Calibrated Preamp Plug-In	Type B	Tektronix
10 Megohm Probe	P6008	Tektronix
Pulse Generator	101	Datapulse
Sweep Oscillator	SD104A	Spectral Dynamics
Volt-Ohmmeter	269	Simpson

4.2. PERIODIC CALIBRATION PROCEDURE

4.2.1 Preliminary Setup

a. Set the SD116 on the test bench and apply power. (Refer to paragraph 2.3 in Section II.) Allow at least a 5-minute warmup period and remove the top chassis cover plate.

b. Set FREQ RANGE switch to 5-5K and X-CAL to OPER.

4.2.2 Power Supply

Use a DVM and oscilloscope, check the d-c voltage and ripple at each of the following terminal points on power supply board A2:

Terminal	D-C Voltage	A-C Ripple
E6	+17V ±2.5V	<4V p-p
-15	-15V ±0.05V	<4 mV p-p
E3	+31V ±3.5V	<4V p-p
+15	+15V ±0.05V	<4 mV p-p

If necessary, adjust A2R11 for -15V ±0.05V, and then A2R2 for +15V ±0.05V, in that order.

On circuit card A1, connect DVM to A1CR12 cathode (bottom lead), and measure +25V ±2V.

NOTE

Throughout the following procedures, the frequency period is given in parenthesis after each calibration frequency.

4.2.3 2-kHz Oscillator

a. Set X-CAL switch to UPPER.

b. Connect frequency counter to A1TP16.

c. Measure 2 kHz ±0.08 Hz (500 µs ±0.25 µs). Adjust A1R27 as necessary for proper frequency.

d. Set X-CAL switch to OPER.

4.2.4 Sample and Hold Circuit

Remove power, remove A1Q18, and Re-apply power. Connect SD104A and frequency counter to INPUT J1. Adjust SD104A for 1 Vrms sine wave output, at frequency of 50 Hz ±0.005 Hz (20 ms ±0.02 ms). Connect DVM to A1TP11.

4.2.4 Sample and Hold Circuit (Cont'd)

a. Adjust A1R58 as necessary for DVM reading of 1V ±10 mV at A1TP11.

b. Change INPUT frequency to 5 kHz ±5 Hz (200 µs ±0.2 us), and adjust A1R65 for 10 mV ±0.1 mV at A1TP11.

c. Because some interaction exists, repeat steps a. and b. as necessary to obtain proper readings.

d. Change input frequency to 5 Hz ±0.005 Hz (200 ms ±0.2 ms); measure 10V ±0.1V. If voltage is incorrect, repeat steps a., b., and d. for "best fit" in-spec readings.

e. Remove power, re-insert A1Q18, and re-apply power.

4.2.5 Log Converter

a. Adjust SD104A for INPUT frequency of 5 Hz ±0.005 Hz (200 ms ±0.2 ms). Connect DVM to A1TP18.

b. Note equal incremental voltage changes between input frequencies of 5 Hz and 50 Hz, 50 Hz and 500 Hz, and 500 Hz and 5 kHz. If necessary, adjust A1R81 for equal incremental voltage changes. 3.20 3,12 3,38 best possible difference

4.2.6 Output Voltage

a. Adjust SD104A for INPUT frequency of 5 kHz ±5 Hz (200 µs ±0.2 µs).

b. Measure 10V ±24 mV at A1TP18. Adjust A1R105 as necessary for proper reading.

c. Adjust SD104A to 5 Hz ±0.005 Hz (200 ms ±0.2 ms).

d. Measure 0V ±24 mV at A1TP18. Adjust A1R94 as necessary for proper reading.

e. Interaction exists between the adjustments of steps b. and d.; repeat steps a. through d. as necessary to obtain proper readings.

4.2.7 Output Linearity Check

Check for the proper d-c voltage at A1TP18 for each of the following frequencies:

4.2.7 Output Linearity Check (Cont'd)

INPUT FREQ (Hz)		PERIOD		VOLTAGE AT 1ATP18
5,000	±5	200 µs	±0.2 µs 10,002	9.976V to 10.024V
1,581	±1.6	632.5 µs	±0.633 µs 8,32	8.309V to 8.357V
500	±0.5	2 ms	±0.002 ms 6,65	6.642V to 6.690V
158.1	±0.16	6.325 ms	±0.0063 ms 5,00	4.976V to 5.024V
50	±0.05	20 ms	±0.02 ms 3,33	3.309V to 3.357V
15.81	±0.016	63.25 ms	±0.0633 ms 1,68	1.642V to 1.690V
5.00	±0.005	200 ms	±0.2 ms +,002	-24 mV to +24 mV

4.2.8 X-CAL Check

a. Set X-CAL switch to UPPER, and measure 8.667V ±50 mV at A1TP18. 8,60

b. Set X-CAL to LINE. Sequentially set FREQ RANGE switch to 5-5k, 10-10k, and 20-20k; and measure 3.6V, 2.6V, and 1.6V (all ±24 mV) respectively at A1TP18. 3,59

4.3 TROUBLESHOOTING

4.3.1 General Checks

Before disassembling the SD116 for circuit troubleshooting, make the following visual checks:

a. Check all external cabling, and check for duplication of input signals and output loading at front and rear panel connectors.

b. Check that the 230/115 line voltage selector switch on the rear panel is set correctly, and that the applied line voltage and frequency are correct.

4.3.2 Power Supply Check

Perform the procedures of paragraphs 4.2.1 and 4.2.2. If the power supply voltages are correct, proceed to the log frequency converter checks of paragraph 4.3.4. If the voltages are not correct, proceed as follows in paragraph 4.3.3.

4.3.3 Power Supply Inoperative

If no power supply voltages are present, check the a-c input circuit.

a. Measure ≈115V ac rms across A2T1 primary windings, between terminals 1 and 2, and 3 and 4 (regardless of POWER IN voltage).

b. Measure +31V ±3.5V at terminal A2E3. If incorrect, check diodes A2CR1 and A2CR2, and capacitor A2C9.

c. Measure +17V ±2.5V at terminal A2E6. If incorrect, check diodes A2CR3 and A2CR4, and capacitor A2C10.

If the voltages measured in steps a., b., and c. are correct, and the +15V and -15V outputs are low, a partial short might exist. Proceed to step d.

d. Remove power, remove the two screws that hold card A1, and remove card A1.

e. With an ohmmeter, check for shorts between the +15V and -15V buses and ground. Using standard troubleshooting techniques, eliminate any possible shorted parts, wiring, etc.

For the following powered checks, load the power supply output; connect a 150 ohm 5%, 2 watt resistor from +15 to GND, and connect a 300 ohm 5%, 1 watt resistor from -15 to GND.

f. Apply power, and check the -15V section for proper operation. Note that the +15V section is slaved to the -15V bus. If the -15V section is operating, proceed to step h.; if not, proceed to step g.

g. Check all voltages on transistors A2Q5, A2Q4, A2Q6, and Q2 (on the heat sink). The three important check points are emitter and base of A2Q4 and collector of A2Q6. (A2Q5 sets reference for A2Q4, A2Q4 controls A2Q6, which in turn controls series regulator Q2 on the heat sink.)

NOTE

If the preceding voltages are not correct and it is suspected that the +15V section is introducing the error, isolate the two sections. Disconnect one end of both resistors A2R3 and A2R4.

After the -15V section has been checked out satisfactorily, reconnect A2R3 and A2R4 (if necessary) and proceed to step h.

4.3.3 Power Supply Inoperative (Cont'd)

h. Check all voltages on transistors A2Q2, A2Q1, A2Q3, and Q1 (on the heat sink). The three important check points are emitter and base of A2Q1 and base of A2Q3. (A2Q2 provides temperature stability for A2Q1. A2Q1 controls A2Q3 which controls series regulator Q1 on the heat sink.)

After the power supply has been satisfactorily checked out and all output voltages are correct, remove power, disconnect the 150 ohm and 300 ohm resistor loads.

CAUTION

To ensure no damage to the power supply circuitry when card A1 is inserted, check card A1 for possible shorts in accordance with the following step i.

i. Measure the resistances between the d-c power buses and ground on circuit card A1.

If a short or very low resistance is found, see the schematic and component layout drawing. Disconnect one end of each part that ties between a d-c power bus and ground until short is eliminated, and thus, the faulty part is found.

After the d-c power buses of circuit card A1 have been checked out satisfactorily, plug it into its socket, and replace the two holding screws. Apply power and again check for correct power supply output voltages.

If the power supply voltages are correct, proceed to paragraph 4.3.4 for log frequency converter card A1 checks.

4.3.4 Log Frequency Converter Card A1

A part failure will normally be indicated by incorrect or the absence of LOG FREQ OUTPUT voltage. The X-CAL switch provides a quick operational check. (See the functional block diagram of Figure 3-2, the associated test point waveforms in Figure 3-1, and the schematic diagram in the back of this manual.) The following steps should help localize a fault to a particular circuit.

a. If applicable, perform the Preliminary Setup procedure of paragraph 4.2.1; ensure that all d-c operating voltages are correct.

b. Set X-CAL switch to LINE and connect DVM to A1TP18. Sequentially set FREQ RANGE switch to 5-5K, 10-10K, and 20-20K; and measure 3.6V, 2.6V, and 1.6V (all ±24 mV) respectively at A1TP18.

4.3.4 Log Frequency Converter Card A1 (Cont'd)

If these voltages are correct, suspect trouble in the external cabling and ancillary equipment in the system. If none of the voltages are correct, perform step c., otherwise proceed to step d.

c. Set X-CAL switch to UPPER and measure 8.667V ±50 mV at A1TP18.

If this voltage is correct, the circuits between A1TP4 and A1TP18 are operating properly; in this case, suspect trouble between A1TP1 and A1TP4 and perform step d.

d. Set X-CAL to LINE. Using standard troubleshooting techniques, check for proper waveforms and voltages between A1TP1 and A1TP4 for each setting of the FREQ RANGE switch.

If the 5-5k FREQ RANGE setting is correct, but the 10-10k or 20-20k do not operate, check the applicable NAND gates and frequency dividing flip-flop(s).

If the UPPER X-CAL output voltage is absent or incorrect, first suspect the 2-kHz oscillator. Perform step e.

e. With X-CAL set to UPPER, connect frequency counter to A1TP16 and measure 2 kHz ±0.08 Hz. This frequency should also be at A1TP4.

If the waveform at A1TP4 is correct, continue checking for proper waveforms at all test points (see Figures 3-1 and 3-2), and for proper voltages (see the schematic diagram) between A1TP4 and A1TP18.

It is sometimes desirable to check the operation of each ramp circuit separately. To disable ramp No. II while checking ramp No. I, remove power, remove A1Q18, and then re-apply power. In like manner, ramp No. II can be checked by removing A1Q24. In either case, be sure to return the transistor to its socket after completion of circuit troubleshooting.

After the trouble has been eliminated, perform the periodic calibration procedure of paragraph 4.2. If the voltages at A1TP18 are out of specification (para 4.2.7), perform the detailed calibration procedure of paragraph 4.5 in its entirety.

4.4 PARTS REPLACEMENT

Except for some special SDC specification-controlled parts listed in Table 4-2, which must be ordered from Spectral Dynamics Corporation, standard electronic parts have been used throughout the instrument. Spectral Dynamics Corporation maintains a complete stock of all parts including complete printed circuit cards.

When ordering a replacement part or assembly, be sure to include the reference designation, the part number or manufacturers designation, and a complete description; include also the instrument name, model number, and serial number.

Table 4-2. SPECIAL REPLACEABLE PARTS LIST.

Ref. Desig.	Description	Part No. or Mfr. Desig.
A1	Log Frequency Converter Circuit Card Assembly	11160-1
A2	Power Supply Circuit Card Assembly	11194-1
M1	FREQ (Hz) Meter	20013-197
Q1,Q2	2N3391A (Factory selected pair)	20013-044A
T1	Power Transformer	20013-101
	Knob, FREQ RANGE (Hz)	20013-176
	Knob, X-CAL	20013-177
	Power Cord	Belden 17258-S

4.5 DETAILED CALIBRATION PROCEDURE

This calibration procedure is the procedure used by the factory during final checkout and calibration of the Model SD116 Log Frequency Converter. The test equipment required is listed in Table 4-1; test equipment having equal or better characteristics may be substituted. See the schematic diagram and component layout drawing in the back of this manual for the location of all calibration controls and test points; note that the test points are identified on the parts side of the circuit card.

4.5.1 Preliminary - POWER OFF Adjustments

a. Mechanically adjust the front panel meter to 5 (bottom scale).

b. Set 115/230 switch on rear of chassis to show proper input line voltage, and accordingly check for proper FUSE (115V ac, ½A SLO BLO; 230V ac, ¼A SLO BLO).

c. Set the FREQ RANGE switch to 5-5K and X-CAL to OPER.

4.5.2 Power Supply

a. Apply power; red POWER switch/indicator should light. Allow a 5-minute warmup period, and remove the top chassis cover plate.

b. Connect DVM and oscilloscope to -15 terminal on circuit card A2. Adjust A2R11 for -15V ±10 mV. Ripple should be <4 mV p-p.

4.5.2 Power Supply (Cont'd)

c. Connect DVM and oscilloscope to +15 terminal on circuit card A2. Adjust A2R2 for +15V ±10 mV. Ripple should be <4 mV p-p.

d. Connect DVM and oscilloscope to A2E6, and measure +17V ±2.5V; ripple <4V p-p.

e. Connect DVM and oscilloscope to A2E3 and measure +31V ±3.5V; ripple <4V p-p.

f. On circuit card A1, connect DVM to A1CR12 cathode (bottom lead) and measure +25V ±2V.

NOTE

Throughout the following procedures, the frequency period is given in parenthesis after each calibration frequency.

4.5.3 2-KHz Oscillator

a. Set X-CAL to UPPER; connect frequency counter to A1TP16.

b. Adjust A1R27 for 2 kHz 0.08 Hz (500 µs ±0.25 µs.)

c. Set X-CAL to OPER.

4.5.4 Sample and Hold Circuits

Remove power, remove A1Q18, and re-apply power. Connect SD104A and frequency counter to INPUT J1. Adjust SD104A for 1 Vrms sine wave output, at frequency of 50 Hz ±0.005 Hz (20 ms ±0.02 ms). Connect DVM to A1TP11.

a. Adjust A1R58 for DVM reading of 1V ±10 mV.

b. Change INPUT frequency to 5 kHz ±5 Hz (200 µs ±0.2 µs), and adjust A1R65 for 10 mV ±0.1 mV.

c. Because some interaction exists, repeat steps a. and b. as necessary to obtain proper readings.

d. Change input frequency to 5 Hz ±0.005 Hz (200 ms ±0.2 ms); measure 10V ±0.1V. If voltage is incorrect, repeat steps a., b., and d. for "best fit" in-spec readings.

e. Re-insert A1Q18.

4.5.5 Ramp Adjust

a. Change INPUT frequency to 50 Hz ±0.05 Hz (20 ms ±0.02 ms), and connect oscilloscope to A1TP11.

4.5.5 Ramp Adjust (Cont'd)

b. Adjust A1R46 for minimum ripple. (This equalizes the amplitudes of ramps I and II.)

c. Again check steps a., b., and d. of paragraph 4.5.4 for in-spec readings.

d. Measure <100 mV p-p ripple at A1TP18.

4.5.6 Log Converter

a. Adjust SD104A for INPUT frequency of 5 Hz ±0.005 Hz (200 ms ±0.2 ms).

b. Adjust A1R81, A1R94, and A1R105 to midrange (approximately 12½ turns from either end).

c. Connect DVM to A1TP18.

d. Note incremental voltage changes as input frequency is changed between 5 Hz and 50 Hz, 50 Hz and 500 Hz, and 500 Hz and 5 kHz. Adjust A1R81 as necessary for equal (±1%) incremental voltage changes.

4.5.7 Output Voltage

a. Adjust SD104A for INPUT frequency of 5 kHz ±5 Hz (200 µs ±0.2 µs).

b. Adjust A1R105 for 10V ±24 mV at A1TP18.

c. Adjust SD104A to 5 Hz ±0.005 Hz (200 ms ±0.2 ms).

d. Adjust A1R94 for 0V ±24 mV at A1TP18.

e. Interaction exists between adjustments of steps b. and d.; repeat steps a. through d. as necessary to obtain proper readings.

4.5.8 Output Linearity

a. Check the d-c voltage at A1TP18 for each of the following frequencies (FREQ RANGE set to 5-5K):

INPUT FREQ (Hz)		PERIOD		VOLTAGE AT A1TP18
5,000	±5	200 µs	±0.2 µs	9.976V to 10.024V
1,581	±1.6	632.5 µs	±0.633 µs	8.309V to 8.357V
500	±0.5	2 ms	±0.002 ms	6.642V to 6.690V
158.1	±0.16	6.325 ms	±0.0063 ms	4.976V to 5.024V
50	±0.05	20 ms	±0.02 ms	3.309V to 3.357V
15.81	±0.016	63.25 ms	±0.0633 ms	1.642V to 1.690V
5.00	±0.005	200 ms	±0.2 ms	-24 mV to +24 mV

4.5.8 Output Linearity (Cont'd)

b. Set FREQ RANGE switch to 10-10K and check the d-c voltage at A1TP18 for each of the following frequencies:

INPUT FREQ (Hz)		PERIOD		VOLTAGE AT A1TP18
10,000	±10	100 µs	±0.1 µs	9.976V to 10.024V
1,000	± 1	1 ms	±0.001 ms	6.642V to 6.690V
100	± 0.1	10 ms	±0.01 ms	3.309V to 3.357V
10	± 0.01	100 ms	±0.1 ms	-24 mV to +24 mV

c. Set FREQ RANGE switch to 20-20K and check the d-c voltage at A1TP18 for each of the following frequencies:

INPUT FREQ (Hz)		PERIOD		VOLTAGE AT A1TP18
20,000	±20	50 µs	±0.05 µs	9.976V to 10.024V
2,000	± 2	500 µs	±0.5 µs	6.642V to 6.690V
200	± 0.2	5 ms	±0.005 ms	3.309V to 3.357V
20	± 0.02	50 ms	±0.05 ms	-24 mV to +24 mV

4.5.9 Wave-Shape Response

a. Insert lab amplifier between SD104A and SD116 INPUT, J1.

b. Adjust SD104A (and lab amplifier) for 500 Hz ±0.5 Hz (2 ms ±0.002 ms) at 0.2V p-p measured at J1.

c. Set FREQ RANGE switch to 5-5K.

d. Check for 6.642V to 6.690V at A1TP18 for sine wave, square wave, and triangular wave inputs.

e. Apply 100V p-p to J1 and repeat step d.

f. Disconnect SD104A and connect pulse generator to lab amplifier input.

g. Adjust pulse generator (and lab amplifier) for 500 Hz ±0.5 Hz, 0.2V p-p, with 30% duty cycle, measured at J1.

h. Check for 6.642V to 6.690V at A1TP18.

i. Change input amplitude at J1 to 100V p-p, and repeat step h.

4.5.9 Wave-Shape Response (Cont'd)

j. Disconnect pulse generator and lab amplifier, and connect SD104A to INPUT J1 of SD116.

4.5.10 Response to Frequency Change

a. On SD116, set FREQ RANGE switch to 5-5k.

b. On SD104A, set MULTIPLIER A to 1 and adjust for 50 Hz ±0.05 Hz.

c. Connect storage oscilloscope to A1TP18 and adjust horizontal sweep for 500 ms/cm.

d. On SD104A, switch MULTIPLIER A to 0.1 and note 10% to 90% response time on oscilloscope; it should be 500 ms $\binom{+200 \text{ ms}}{-300 \text{ ms}}$

4.5.11 X-CAL

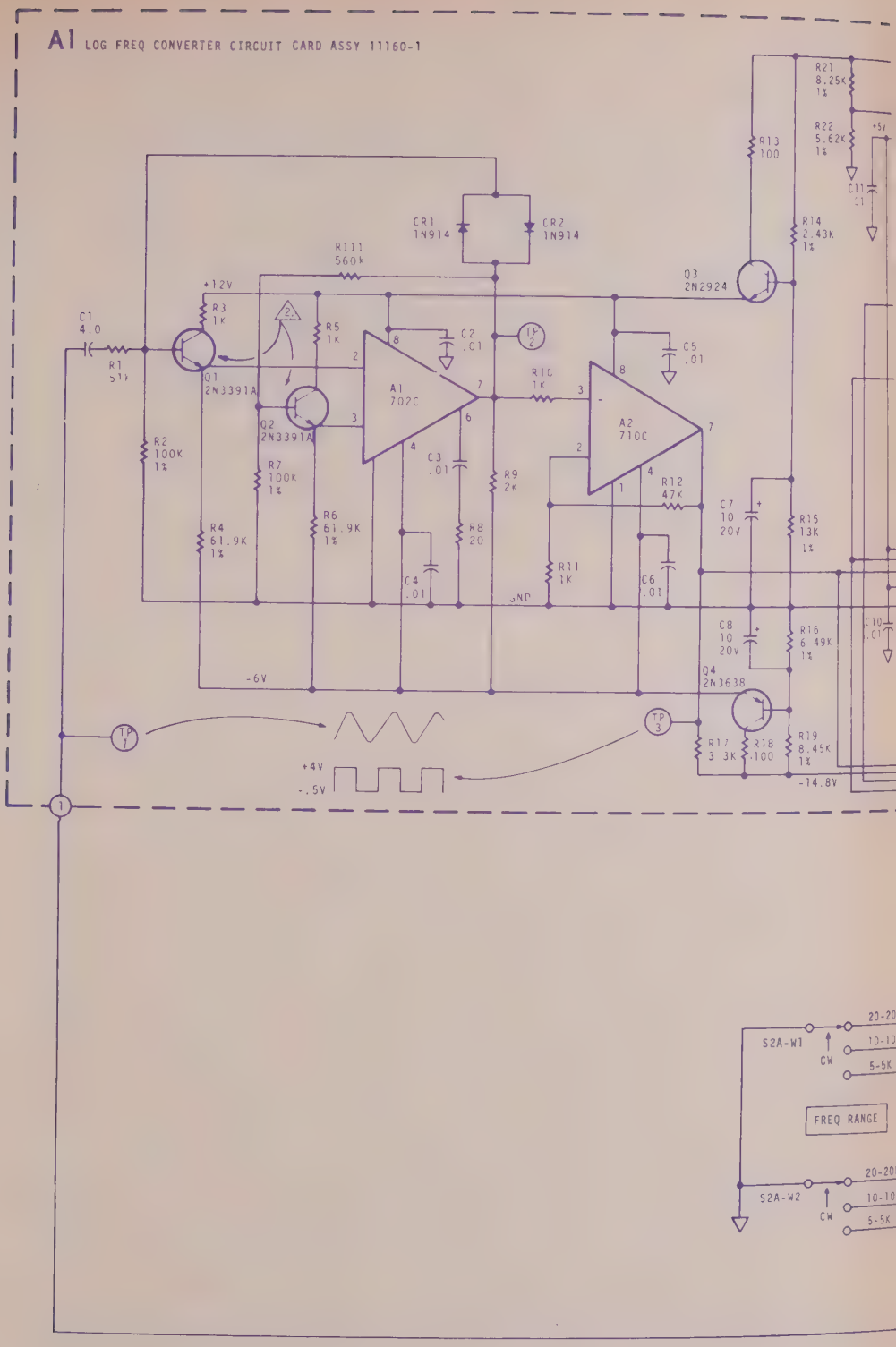
a. Set X-CAL switch to UPPER, and measure 8.667V ±50 mV at A1TP18.

b. Set X-CAL to LINE. Sequentially set FREQ RANGE switch to 5-5k, 10-10k, and 20-20k; and measure 3.6V, 2.6V, and 1.6V (all ±34 mV) respectively at A1TP18.

4.5.12 Meter Calibration

a. On SD104A, adjust frequency for 10 kHz.

b. On SD116, set FREQ RANGE switch to 10-10K and then adjust R1 (FULL SCALE METER ADJ located on small circuit card mounted on rear of frequency meter) for a full scale meter indication (10 kHz).



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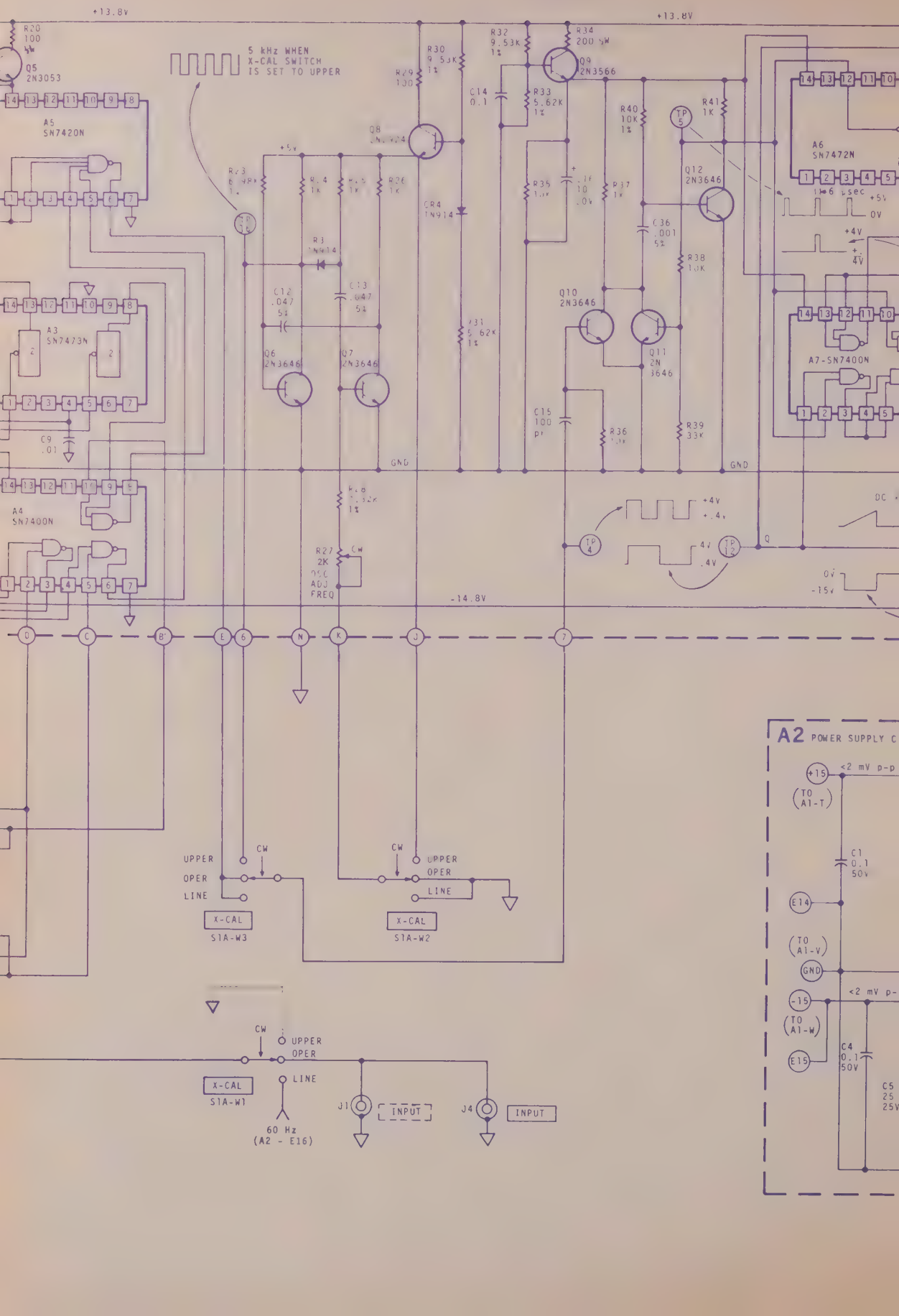
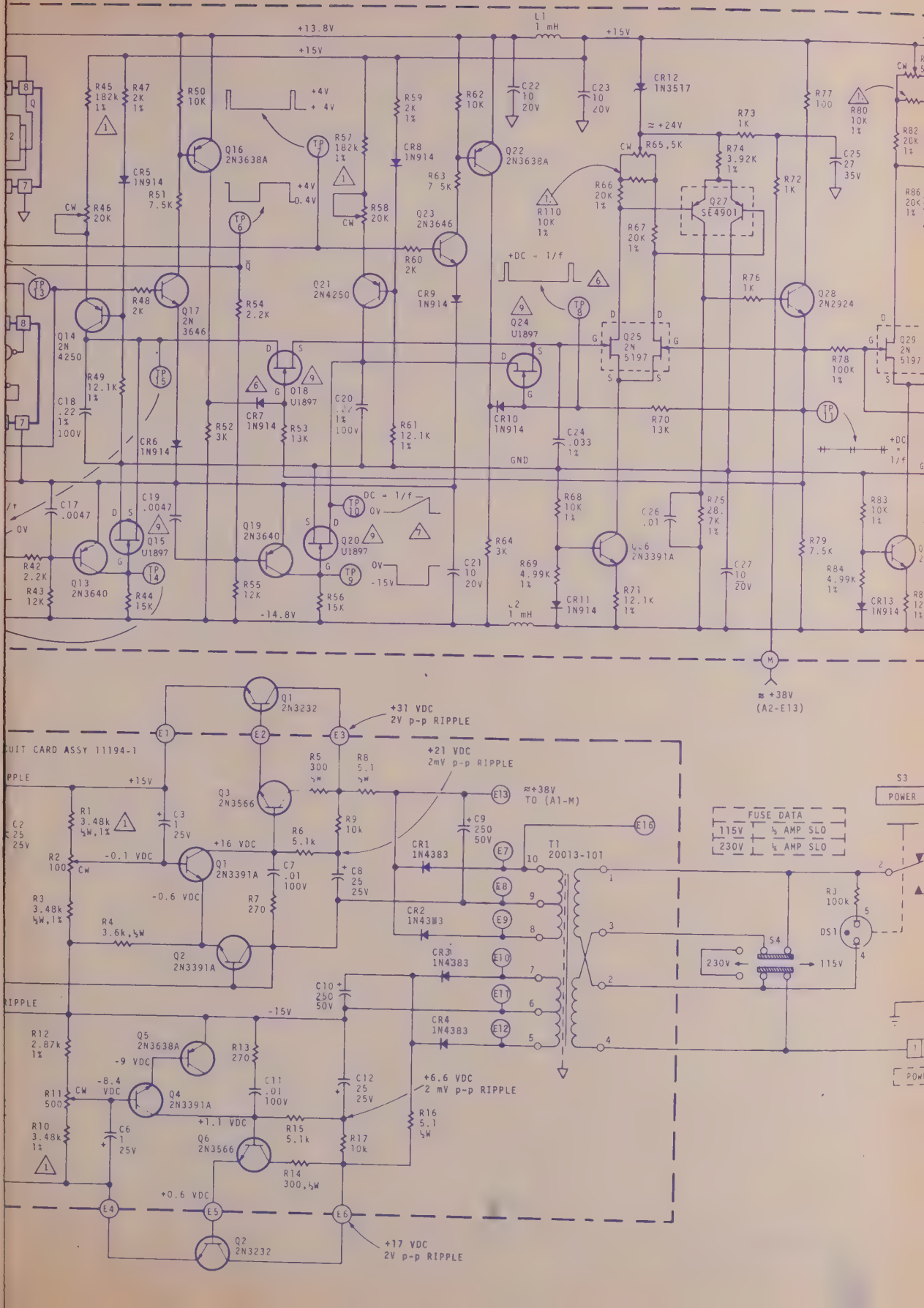
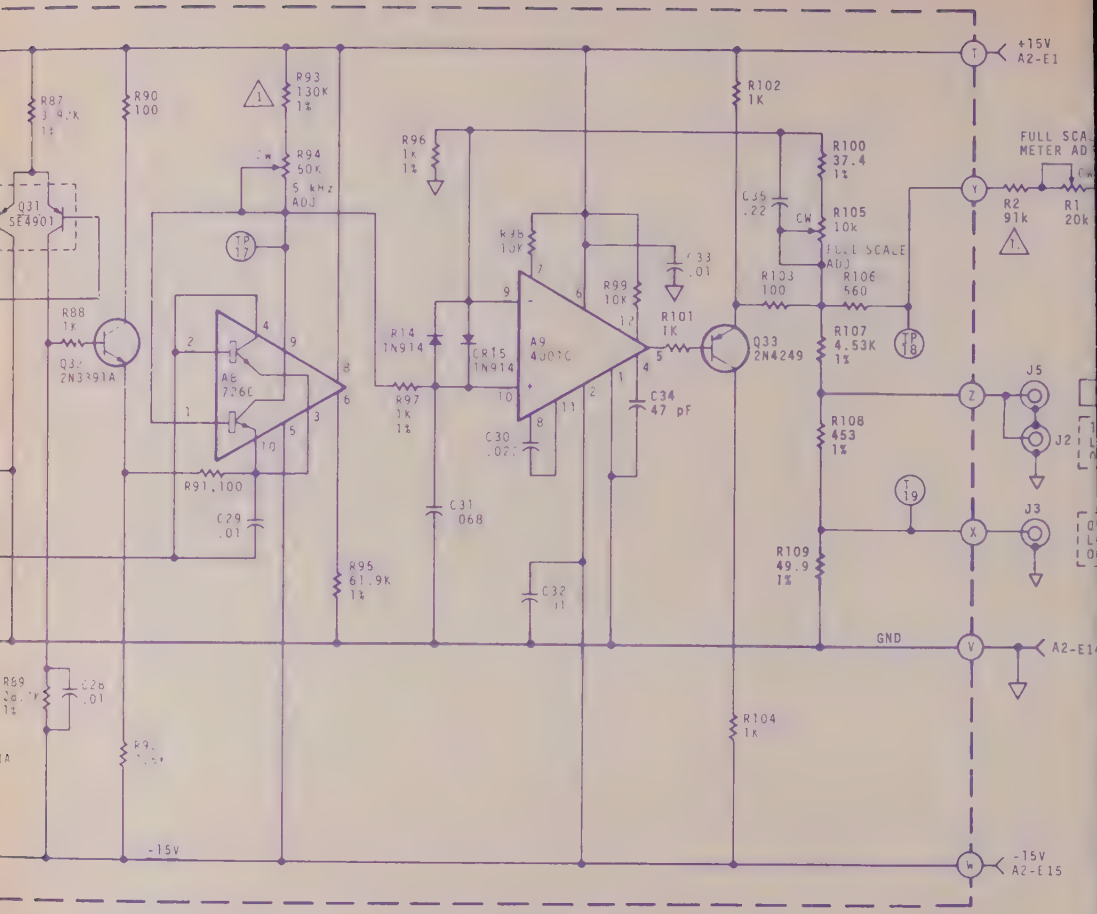
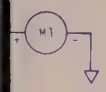

+13.8v
+13.8V
5 kHz WHEN
X-CAL SWITCH
IS SET TO UPPER
A5
SN7420N
A3
SN7473N
A4
SN7400N
A6
SN7472N
A7-SN7400N
Q5
2N3053
Q8
Q9
2N3566
Q10
2N3646
Q11
2N
3646
Q12
2N3646
Q6
2N3646
Q7
2N3646
CR4
1N914
R20
100
R30
9.53K
1%
R32
9.53K
1%
R34
200 W
R29
100
C14
0.1
R33
5.62K
1%
R40
10K
1%
R41
1K
TP
5
R35
1.0K
R37
1K
C36
.001
5%
R38
1.0K
C12
.047
5%
C13
.047
5%
R31
5.62K
1%
C15
100
pf
R36
R39
33K
C9
.01
GND
GND
R28
1.62K
1%
R27
2K
CW
ADJ
FREQ
-14.8V
+4V
.4V
TP
4
TP
Q
+4V
0V
-15v
1 to 6 μsec
+5V
0V
+4V
.4V
UPPER
OPER
LINE
CW
X-CAL
S1A-W3
CW
UPPER
OPER
LINE
X-CAL
S1A-W2
CW
UPPER
OPER
LINE
X-CAL
S1A-W1
60 Hz
(A2 - E16)
J1
INPUT
J4
INPUT
A2 POWER SUPPLY C
+15
<2 mV p-p
(TO
A1-T)
C1
0.1
50v
E14
(TO
A1-V)
GND
-15
<2 mV p-
(TO
A1-W)
E15
C4
0.1
50V
C5
25
25V


+13.8V
+15V
L1
1 mH
R45 182k 1%
R47 2K 1%
R50 10K
R46 20K
CR5 1N914
R51 7.5K
Q16 2N3638A
+4V
+ 4V
+4V
0.4V
R57 182k 1%
R58 20K
R59 2K 1%
R62 10K
CR8 1N914
R63 7.5K
Q22 2N3638A
Q23 2N3646
R60 2K
C22 10 20V
C23 10 20V
CR12 1N3517
≈ +24V
R65,5K
R66 20K 1%
R67 20K 1%
R110 10K 1%
R73 1K
R74 3.92K 1%
Q27 SE4901
R72 1K
R77 100
R80 10K 1%
R82 20K 1%
C25 27 35V
R86 20K 1%
R48 2K
Q17 2N 3646
Q14 2N 4250
R54 2.2K
Q21 2N4250
CR9 1N914
+DC ∝ 1/f
Q24 U1897
R76 1K
Q28 2N2924
R49 12.1K 1%
C18 .22 1% 100V
CR6 1N914
R52 3K
Q18 U1897
CR7 1N914
R53 13K
C20 .47 1% 100V
R61 12.1K 1%
CR10 1N914
C24 .033 1%
R70 13K
Q25 2N 5197
Q29 2N 5197
R78 100K 1%
+DC ∝ 1/f
GND
C17 .0047
C19 .0047
Q15 U1897
Q13 2N3640
R42 2.2K
R43 12K
R44 15K
Q19 2N3640
Q20 U1897
DC ∝ 1/f
0V
-15V
R55 12K
R56 15K
-14.8V
C21 10 20V
R64 3K
R68 10K 1%
R69 4.99K 1%
Q26 2N3391A
C26 .01
R75 28.7K 1%
C27 10 20V
R71 12.1K 1%
CR11 1N914
L2 1 mH
R79 7.5K
R83 10K 1%
R84 4.99K 1%
CR13 1N914
≈ +38V
(A2-E13)
Q1 2N3232
+31 VDC
2V p-p RIPPLE
+21 VDC
2mV p-p RIPPLE
R5 300 ½W
R8 5.1 ½W
≈+38V
TO (A1-M)
Q3 2N3566
R1 3.48k ½W,1%
C3 1 25V
C9 250 50V
R6 5.1k
R9 10k
+16 VDC
-0.1 VDC
Q1 2N3391A
C7 .01 100V
C8 25 25V
CR1 1N4383
T1 20013-101
R2 100
R3 3.48k ½W,1%
-0.6 VDC
R7 270
R4 3.6k,½W
Q2 2N3391A
CR2 1N4383
CR3 1N4383
CR4 1N4383
C10 250 50V
-15V
R12 2.87k 1%
Q5 2N3638A
R13 270
-9 VDC
-8.4 VDC
R11 500
Q4 2N3391A
C11 .01 100V
C12 25 25V
+6.6 VDC
2 mV p-p RIPPLE
R10 3.48k 1%
C6 1 25V
+1.1 VDC
R15 5.1k
R16 5.1 ½W
Q6 2N3566
R17 10k
R14 300,½W
+0.6 VDC
Q2 2N3232
+17 VDC
2V p-p RIPPLE
FUSE DATA
115V ⅓ AMP SLO
230V ⅛ AMP SLO
S3
POWER
R3 100k
DS1
S4
230V
115V


+15V
A2-E1
R102
1K
R100
37.4
1%
R96
1K
1%
R93
130K
1%
R94
50K
5 kHz
ADJ
R87
3.9K
1%
R90
100
Q31
5E4901
R88
1K
Q32
2N3391A
A6
726C
R91
100
C29
.01
R95
61.9K
1%
C31
068
R14
1N914
CR15
1N914
R97
1K
1%
C30
.02
A9
4007C
R99
10K
1%
C33
.01
R101
1K
Q33
2N4249
C34
47 pF
C32
.1
R105
10k
FULL SCALE
ADJ
R103
100
R106
560
R107
4.53K
1%
R108
453
1%
R109
49.9
1%
R104
1K
C35
.22
R2
91k
R1
20k
FULL SCALE
METER ADJ
J5
J2
J3
GND
A2-E14
-15V
A2-E15
-15V



REVISIONS						
REV	ECO	S N	DESCRIPTION	DRAFT	CHECK	APP'D
B	489	020	Redrawn. Changed A1R45 & A1R57 to fact. adj. w/o Optimum value 182k. Changed A1R93, A2R1 & A2R10 to fact. adj.	bac 7-1-68		
C	509	065	A1Q15, A1Q18, A1Q20 & A1Q24 WERE 2N4391 AND ADDED NOTE 9.			
D	541	011	A1R27 WAS 1K, A1R28 WAS 7.15K AND A1C12 & A1C13 WERE .02, 1%			
E	547	031	C36 was 1%. C18 & C20 were 50V.			
F	620	→	Add R111 - S/N 011 & on. R105 was 5k. 10k eff. S/N 033, 036, & on.			
G	682	036	INCORP ECO ADDING GRD AT SIA-WI			

NOTES.

1. FACTORY ADJUST COMPONENT WITH OPTIMUM VALUE SHOWN.
2. MATCHED PAIR PER SDC SPEC 20013-044A.
3. UNLESS OTHERWISE SPECIFIED, ALL RESISTOR VALUES ARE IN OHMS WITH CARBON RESISTORS @ ¼W, 5% AND PRECISION RESISTORS @ 1/8W. CAPACITOR VALUES ARE IN MICROFARADS @ 200V, 10%.
4. SYMBOL ▭ INDICATES FRONT PANEL LOCATION;
   SYMBOL ⬚ INDICATES REAR CHASSIS LOCATION.
5. ALL WAVEFORM VOLTAGES ARE NOMINAL.
6. TP8 and Q18-G (SEE FIGURE 3-1 IN SECTION III.)
7. TP10 AND TP15 7V @ 5 Hz, 10 mV ±5 kHz measured with 10 MEGOHM PROBE.
8. TRANSISTORS Q1 & Q2, TYPE 2N3232, ARE MOUNTED ON HEAT SINKS LOCATED ON THE CHASSIS CIRCUIT PLATE.
9. 2N4391 IS A SUBSTITUTE FOR U1897.

HIGHEST REFERENCE DESIGNATORS USED															
ASSEMBLY	A	C	CR	DS	F	J	L	M	Q	R	S	T	TP	E	
11160-1	9	36	15				2		33	111			19		
11194-1		12	4						6	17		1		16	
INTER CONN	2			1	1	6		1	2	3	4				

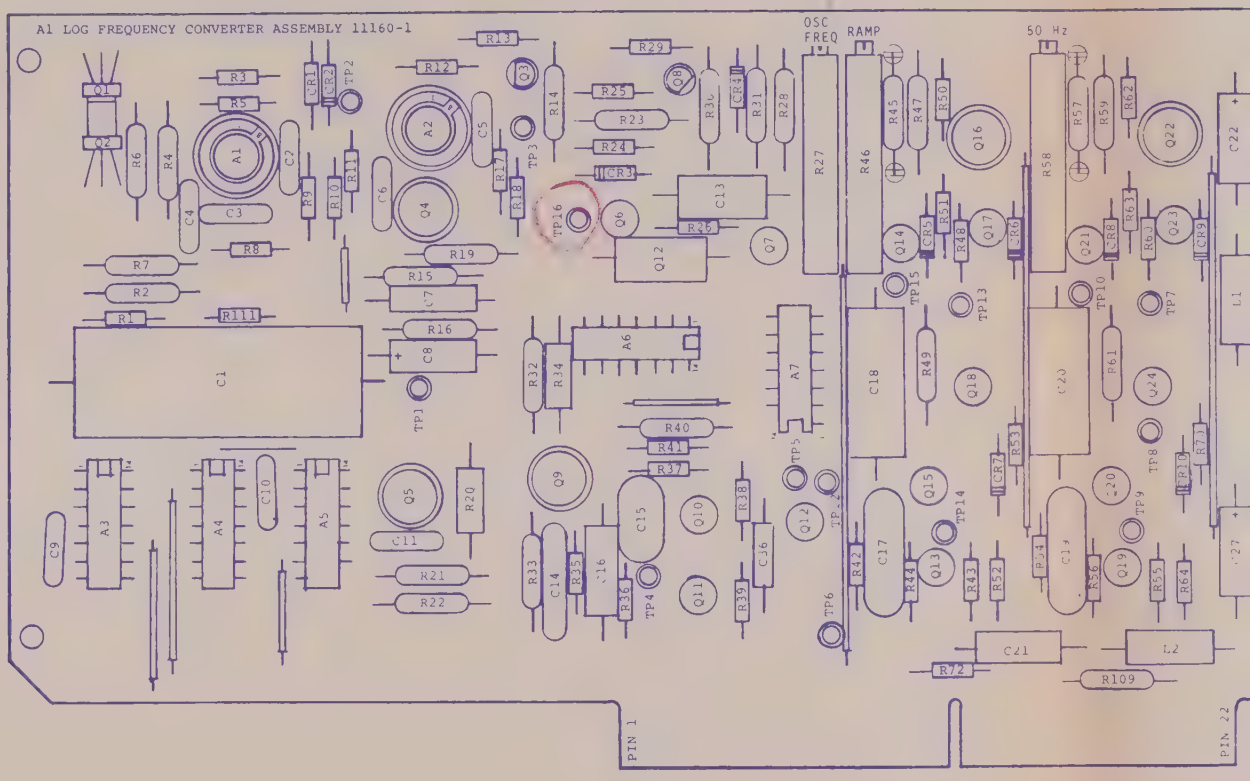
SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO

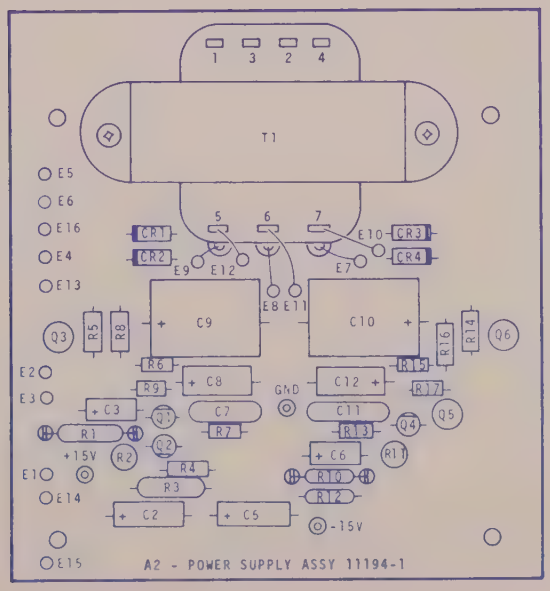
TITLE: SCHEMATIC — Model SD116 Log Frequency Converter

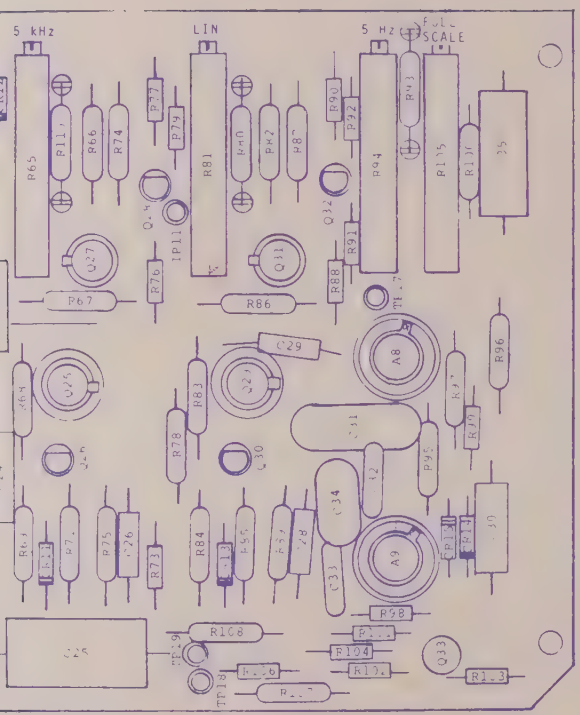
DRAWN	G. B. Clare	
CHECKED	[illegible]	7-8-68
ENGINEER	[illegible]	7-8-68
APPROVED		

SIZE | DRAWING NO 11201 | REV G

SCALE | 7-1-68 | SHEET 1 OF 2


A1 LOG FREQUENCY CONVERTER ASSEMBLY 11160-1
OSC FREQ
RAMP
50 Hz
PIN 1
PIN 22


T1
A2 - POWER SUPPLY ASSY 11194-1
+15V
-15V
GND



REVISIONS						
REV	ECO	S N	DESCRIPTION	DRAFT	CHECK	APP'D
			SEE SHEET ONE.			

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SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO

DRAWN	G. B. Clare	
CHECKED	[signature]	7-8-68
ENGINEER	[signature]	7-8-68
APPROVED	[signature]	7-9-68

TITLE

COMPONENT LAYOUT –

Model SD116 Log Frequency Converter

SIZE	DRAWING NO.	REV
	11201	G
SCALE 7-1-68	SHEET 2 OF 2	